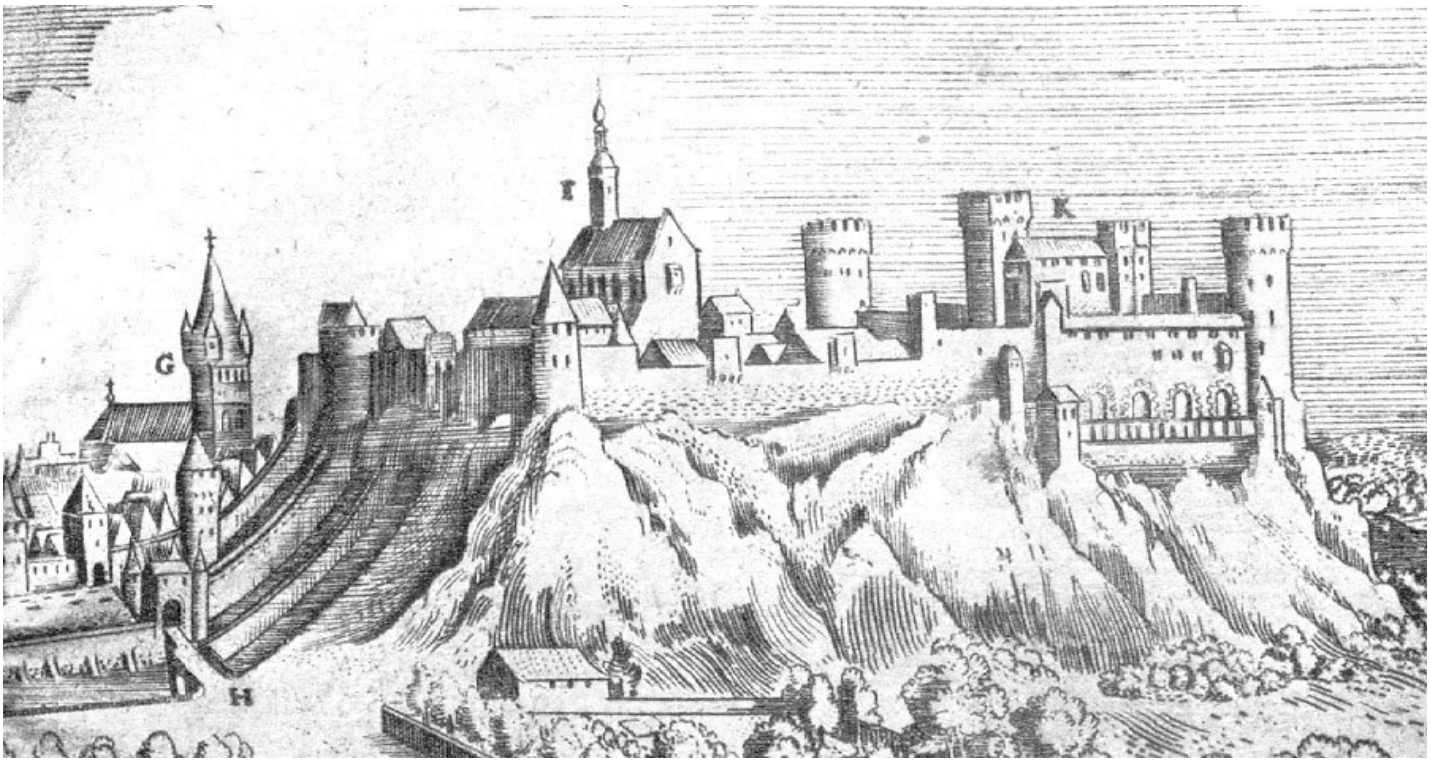
FPL'98

UNIVERSITY OF KAISERSLAUTERN

Eighth International Workshop on

Field-Programmable Logic and Applications

CONFERENCE PROGRAM



August 31 - September 3
Tallinn, Estonia

About the Event

Objectives

The methodology of reconfigurable circuits and systems is evolving from tinkertoy approach to an Innovative Parallel Computing Paradigm which combines computing in time with computing in space. The aim of this workshop is to bring together workers from throughout the world for a wide ranging discussion of all forms of field programmable logic, particularly field programmable gate arrays and complex programmable logic devices, and their applications. It is intended to discuss the increasing range of device types, industrial applications, advanced design tool development, research applications, novel system architectures and educational experiences. The workshop was organized by the Tallinn Technical University and the University of Kaiserslautern as continuation of seven already held workshops in Oxford (1991, 1993 and 1995), Vienna (1992), Prague (1994), Darmstadt (1996) and London (1997).

Conference Survey

Sunday, Aug. 30 at 20.00 in the evening:

Informal Gathering and Registration at the Hotel Viru (lobby), Viru väljak 4, Tallinn

Monday, Aug. 31	Tuesday, Sept. 1	Wednesday, Sept. 2	Thursday, Sept. 3
8.00 - 9.00 *Registration*	8.30 - 10.10 *Session 4:* Development Methods	8.30 - 9.45 *Session 10:* System Development	8.30 -12.00 *Tutorial at Tallinn Technical University:* A Survey of Reconfigurable Computing Architectures, Part 1
9.00 - 9.20 *Opening Session*	10.10 - 10.35 Coffee Break	9.45 - 10.00 Coffee Break	
9.20 - 10.20 Keynote	10.35 - 11.50 *Session 5:* Accelerators	10.00 - 11.40 *Session 11:* Algorithms on FPGAs ---------- 10.00 - 11.15 Poster Introduction	
10.20 - 10.35 Coffee Break	11.50 - 13.05 *Session 6:* System Architectures		
10.35 - 12.15 *Session 1:* Design Methods	13.05 - 14.20 Lunch	11.15 - 12.00 *Session 12:* Poster Exhibition	
12.15 - 13.30 Lunch	14.20 - 16.00 *Session 7:* Applications ---------- 14.20 - 15.35 Poster Introduction	12.00 - 13.00 *Closing session*	13.00 -16.00 *Tutorial at Tallinn Technical University:* A Survey of Reconfigurable Computing Architectures, Part 2
13.30 - 15.10 *Session 2:* General Aspects			
15.10 - 15.30 Coffee Break	15.35 - 16.20 *Session 8:* Poster Exhibition	14.00 - 21.30 Tour to Lahemaa National Park, visiting manors, dinner at Viitna tavern and village party	
15.30 - 17.10 *Session 3:* Prototyping / Simulation	16.20 - 16.40 Coffee Break		
	16.40 - 18.00 *Session 9:* Hardware/Software Codesign		
18.30 Reception at Tallinn Town Hall	19.30 Banquet at von Glehn‘s Castle		

TECHNICAL PROGRAM

Monday, August 31

8.00 - 9.00 **Registration at Tallinn National Library**

9.00 - 9.20 **Opening Session**

9.20 - 10.20 **Keynote**

V.Milutinovic, University of Belgrade:
Key Issues in Reconfigurable Computing

10.20 - 10.35 **Coffee Break**

10.35 - 12.15 **Session 1:** ***Design Methods***

D.Robinson, P.Lysaght, G.McGregor, U Strathclyde:
New CAD Framework Extends Simulation of Dynamically Reconfigurable Logic

W.Luk, S.McKeever, IC London:
Pebble: A Language For Parametrised and Reconfigurable Hardware Design

V.Sklyarov, R.Sal Monteiro, N.Lau, A.Melo, A.Oliveira, K.Kondratjuk, Aveiro U:
Integrated Development Environment for Logic Synthesis of Digital Circuits Based on Dynamically Reconfigurable FPGAs

R.Hartenstein, M.Herz, F.Gilbert, U Kaiserslautern:
Designing for the Xilinx XC6200 FPGAs

12.15 - 13.30 **Lunch**

13.30 - 15.10 **Session 2:** ***General Aspects***

J.Becker, A.Kirschbaum, F.-M.Renner, M.Glesner, TU Darmstadt:
Perspectives of Reconfigurable Computing in Research, Industry and Education

G.Brebner, U Edinburgh:
Field-Progammable Logic: Catalyst for New Computing Paradigms

W.Luk, N.Shirazi, P.Y.K.Cheung, IC London:
Run-time management of partially-reconfigurable designs

M.Platzner, G.De Micheli, Stanford U:
Acceleration of Satisfiability Algorithms by Reconfigurable Hardware

15.10 - 15.30 **Coffee Break**

15.30 - 17.10 **Session 3:** ***Prototyping / Simulation***

J.Stohmann, K.Harbich, M.Olbrich, E.Barke, U Hannover:
An Optimized Design Flow for Fast FPGA-Based Rapid Prototyping

H.Krupnova, G.Saucier, INP Grenoble:
A Knowledge-Based System for Prototyping on FPGAs

R.Macketanz, W.Karl, TU Munich:
JVX - A Rapid Prototyping System Based on Java and FPGAs

J.Shetler, B.Hemme, C.Yang, C.Hinsz, Cal Poly:
Prototyping New ILP Architectures Using FPGAs

18.30 **Reception at Tallinn Town Hall**

Tuesday, September 1

8.30 - 10.10 **Session 4:** ***Development Methods***

Samary Baranov, Ben Gurion U Negev:
CAD System for ASM and FSM Synthesis

J.M.Emmert, A.Randhar, D.Bhatia, U Cincinnati:
Fast Floorplanning for FPGAs

M.Renovell, J.M.Portal, J.Figueras, Y.Zorian, LIRMM-UM2:
SRAM-Based FPGAs: A Fault Model for the Configurable Logic Modules

G.Haug, W.Rosenstiel, FZI Karlsruhe:
Reconfigurable Hardware as Shared Resource in Multipurpose Computers

10.10 - 10.35 **Coffee Break**

10.35 - 11.50 **Session 5:** ***Accelerators***

S.Robinson, M.Caffrey, M.Dunham, LANL
Reconfigurable Computer Array: The Bridge Between High Speed Sensors and Low Speed Computing

W.Luk, P.Andreou, N.Shirazi, D.Siganos, IC London:
A Reconfigurable Engine for Real-Time Video Processing

F.-M.Renner, J.Becker, M.Glesner, TU Darmstadt:
An FPGA Implementation of a Magnetic Bearing Controller for Mechatronic Applications

11.50 - 13.05 **Session 6:** ***System Architectures***

R.Hartenstein, M.Herz, T.Hoffmann, U.Nageldinger, U Kaiserslautern:
Exploiting contemporary memory techniques in reconfigurable accelerators

A.Donlin, U Edinburgh:
Self Modifying Circuitry - A Platform for Tractable Virtual Circuitry

K. GajjalaPurna, K.Simha, D.Bhatia, U Cincinnati:
REACT: Reactive Environment for Runtime Reconfiguration

13.05 - 14.20 **Lunch**

14.20 - 16.00 **Session 7:** ***Applications***

S.Charlwood, P.James-Roxby, U Birmingham:
Evaluation of the XC6200-series architecture for cryptographic applications

A.Zakerolhosseini, P.Lee, E.Horne, U Kent:
An FPGA based object recognition machine

G.Acher, W.Karl, M.Leberecht, TU Munich:
PCI-SCI Protocol Translations: Applying Microprogramming Concepts to FPGAs

T.Callahan, J.Wawrzynek, UC Berkeley
Instruction-Level Parallelism for Reconfigurable Computing

14.20 - 15.35 **Poster Introduction (parallel to S.7)**

15.35 - 16.20 **Session 8:** ***Poster Exhibition***

N.L.Miller, S.F.Quigley, U Birmingham:
A Novel Field Programmable Gate Array Architecture for high speedarithmetic processing

D.MacVicar, S.Singh, XILINX:
Accelerating DTP with Reconfigurable Computing Engines

C.N.Ojeda-Guerra, R.Esper-Chain, M.Estupinan, A.Suarez, U Las Palmas:
Hardware Mapping of a Parallel Algorithm for Matrix-Vector Multiplication

G.Brebner, U Edinburgh:
An Interactive Datasheet for the Xilinx XC6200

N.Woolfries, P.Lysaght, S.Marshall, G.McGregor, D.Robinson, U Strathclyde:
Fast Adaptive Image Processing in FPGAs using Stack Filters

(Continued) **Session 8:** ***Poster Exhibition***

S.Sawitzki, A.Gratz, R.Spallek, U Dresden:
Increasing Microprocessor Performance with Tightly-Coupled Reconfigurable Logic Arrays

N.Bergmann, P.Sutton, Queensland U:
A High-Performance Computing Module for a Low Earth Orbit Satellite using Reconfigurable Logic

S.Yamagiwa, M.Ono, T.Yamazaki, P.Kulkasem, M.Hirota, K.Wada, U Tsukuba:
Maestro-Link: A High Performance Interconnect for PC Cluster

T.Shiozawa, K.Oguri, K.Nagami, H.Ito, R.Konishi, N.Imlig, NTT:
A Hardware Implementation of Constraint Satisfaction Problem Based on New Reconfigurable LSI Architecture

P.Merino, J.Lopez, M.Jacome, U Politecnica de Madrid:
A Hardware Operating System for Dynamic Reconfiguration of FPGAs

E.Cerro-Prada, P.B.James-Roxby, U Birmingham:
High speed low level image processing on FPGAs using distributed arithmetic

T.-T.Do, H.Kropp, C.Reuter, P.Pirsch, U Hannover:
A Flexible Implementation of High-Performance FIR Filters on Xilinx FPGAs

I.Vassanyi, U Veszprem:
Implementing processor arrays on FPGAs

S.Holmstrom, K.Sere, Abo Akademi U:
Reconfigurable Hardware - A Study in Codesign

C.Ackad, TU Braunschweig:
Statechart-based HW/SW-Codesign of a Multi-FPGA-Board and a Microprocessor

16.20 - 16.40 **Coffee Break**

16.40 - 18.00 **Session 9:** ***Hardware/Software Codesign***

G.McGregor, D.Robinson, P.Lysaght, U Strathclyde:
A Hardware/Software Co-design Environment for Reconfigurable Logic Systems

K.Bondalapati, V.Prasanna, U of Southern California:
Mapping Loops onto Reconfigurable Architectures

S.Asaad, K.Warren, IBM T.J.Watson Research Center:
Speed Optimization of the ALR circuit using an FPGA with embedded RAM: A Design Experience

19.30 **Banquet at von Glehn's Castle**

Wednesday, September 2

8.30 - 9.45 **Session 10:** ***System Development***

R.Kress, A.Pyttel, A.Sedlmeier, Siemens AG:
High-level Synthesis for Dynamically Reconfigurable HW/SW-Systems

N.McKay, S.Singh, XILINX:
Dynamic Specialisation of XC6200 FPGAs by Partial Evaluation

S.Guccione, XILINX:
Webscope: A Circuit Debug Tool

9.45 - 10.00 **Coffee Break**

10.00 - 11.40 **Session 11:** ***Algorithms on FPGAs***

D.Lavenier, Y.Saouter, IRISA-CNRS:
Computing Goldbach partitions using pseudo-random bit generator operators on a FPGA systolic array

P.Zhong, M.Martonosi, S.Malik, P.Ashar, Princeton U:
Solving Boolean Satisfiability with Dynamic Hardware Configurations

J.Põldre, M.Mandre, K.Tammemäe, Tallinn Technical U:
Modular exponentiator realization on FPGA

B.Feher, G.Szedo, TU Budapest:
Cost effective 2x2 inner product processors

10.00 - 11.15 **Poster Introduction (parallel to S.11)**

11.15 - 12.00 **Session 12:** ***Poster Exhibition***

A.Touhafi, W.F.Brissinck, E.F.Dirkx, U Brussel:
Simulation of ATM switches using Dynamically Reconfigurable FPGA's

T.Rissa, T.Mäkeläinen, J.Siirtola, J.Niittylahti, Tampere U:
Fast Prototyping Using System Emulators

A.Dandalis, V.Prasanna, U of Southern California:
Space-efficient Mapping of 2D-DCT onto Dynamically Configurable Coarse-Grained Architectures

I.Lemberski, M.Ratniece, Riga Aviation U:
XILINX4000 Architecture-Driven Synthesis for Speed

V.Tomachev, Inst. of Eng. Cybernetics Belarus:
The PAL-implementation of Boolean function characterized by minimum delay

A.Abo Shosha, P.Reinhart, F.Rongen, Research Centre Jülich:
Reconfigurable PCI-Bus Interface (RPCI)

A.Trost, A.Zemva, B.Zajc, U Ljubljana:
Programmable Prototyping System for Image Processing

J.Fischer, C.Müller, H.Kurz, TU Aachen:
A Co-Simulation Concept for an Efficient Analysis of Complex Logic Designs

A.Döring, W.Obelöer, G.Lustig, Med. U Lübeck:
Programming and Implementation of Reconfigurable Routers

M.Moure, U Vigo:
Virtual Instruments based on reconfigurable logic

C.Siemers, D.Möller, FH Westküste:
The >S<puter: Introducing a Novel Concept for Dispatching Instructions Using Reconfigurable Hardware

L.Lagadec, B.Pottier, U de Bretagne Occidentale:
A 6200 model and editor based on object technology

M.Eisenring, J.Teich, ETH Zürich:
Interfacing Hardware and Software

J. Hwang, E. Dellinger, S. Mitra, S. Mohan, C. Patterson, R. Wittig, XILINX:
Generating Layouts for Self-Implementing Modules

12.00 - 13.00 **Closing Session**

T.Maruyama, T.Funatsu, T.Hoshino, U of Tsukuba:
A Field-Programmable Gate-Array System for Evolutionary Computation

T.Miyazaki, K.Shirakawa, M.Katayama, T.Murooka, A.Takahara, NTT:
A Transmutable Telecom System

Conclusions, Award Ceremony and Announcements

14.00 - 21:30 **Tour to Lahemaa National Park, visiting manors, dinner at Viitna tavern and village party**

Thursday, September 3

8.30 - 12.00 **Tutorial at Tallinn Technical University**

B. Radunovic, V. Milutinovic, Univ. Belgrade:
A Survey of Reconfigurable Computing Architectures, Part 1

13.00 - 16.00 **Tutorial at Tallinn Technical University**

B. Radunovic, V. Milutinovic, Univ. Belgrade:
A Survey of ReconfigurableComputing Architectures, Part 2

Paper abstract

In this paper, a survey of reconfigurable computing is presented. There have been other surveys in this field, but none as exhaustive as this one tries to be. The main goal of this paper is to consider a large variety of different approaches to the field of reconfigurable computing, and to make a thorough classification. This classification is aimed at helping the understanding of the current systems, as well as the development of new systems. We first define the classification criteria and the classification itself. Each class is described briefly. Next, we classify the existing systems, based on their dominating characteristic, and finally we list each surveyed system under one of the classification classes. Each presented example is described using the same template (authors, essence of the approach and details of interest, advantages and drawbacks).

Place

The Workshop will be held at the National Library of Estonia, Tõnismägi 2, Tallinn, Estonia, from August 31st to September 3rd, 1998.

Language

The official language of the workshop is English. It will be used for all printed materials, presentations and discussions.

Proceedings

The proceedings are published by Springer-Verlag in the series „Lecture Notes in Computer Science“ and distributed at the conference. Additional copies may be ordered directly from Springer-Verlag.

Workshop Committee

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Steve Trimberger, Xilinx, USA

Conference Hotline

IN CASE OF ANY PROBLEMS DURING THE CONFERENCE PLEASE CONTACT (FROM AUG. 15 TO SEPT. 4)

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