# List of FPGA-based Computing Machines

Welcome to the list of FPGA-based computing machines. This list was first compiled in the beginning of 1994, where there were a small handful of FPGA boards available. Since then the number has grown considerably. Because of the large and growing number of FPGA-based systems currently available, I have decided to stop making additions to this list and leave it available as an historical document. The last entry added to this list was in March 1999. Other more up to date places to find a variety of FPGA-based hardware are available. I suggest Optimagic's Programmable Logic Jump Station as a good resource.

I have also re-ordered the entries grouped by type of device used. This provides a rough chronological order of introduction of these boards. The original list, sorted alphabetically, is still available.

Finally, thanks again to everyone who has contributed to this list.

*List of FPGA-based Computing Machines / Steve Guccione / **guccione@nospam.io.com***
*Last updated: 21 August 2000*

*Return to Steve Guccione's home page*

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**Actel:**

- Windchime (Actel 1020A)

**Algotronix CAL Series:**

- Chameleon
- CHS 2x4
- SPACE

**Altera:**

- ARC-PCI (EPF10K50)
- epX31 (EPX780)
- ipEngine-1 (EPF6016)
- MSP0 (EPF10K100)
- RIPP (FLEX 81188)
- RIPP10 (FLEX 81188)
- TM-2 (EPF10K50)
- VIP (FLEX 81500)

**ATT / Lucent /Lattice ORCA:**

- Cheops
- SLC1655 (OR2CA15)

**Intel:**

- nfXboard (NFX780)
- Stack (iFX780)

**Xilinx XC3000 Series:**

- Accelerator (XC3195)
- Anyboard (XC3042)
- ArMen (XC3090)
- BORG (XC3042)
- DSP-56X (XC3042)
- The Flexible Processor (XC3020)
- GANGLION (XC3090)
- HARP-1 (XC3195)
- Mushroom (XC3090)
- nP (XC3090)
- perle-0 (XC3020)

**Xilinx XC4000 Series:**

- ACME (XC4010)
- APS X-84 (XC4000 / XC5000)
- BORG II (XC4003)
- CHAMP (XC4013)
- 9204/FPGA/DS-link (XC4025EX)
- Distributed Virtual Computer (XC4013E)
- EDgAR-2 (XC4013XLT)
- ENABLE++ (XC4013)
- EVC (XC4010)
- EVC1 Virtual Computer (XC4013E)
- Functional Memory Computer (XC4010)
- G-800 (XC4010)
- G-900 (XC4028EX)
- ISA Proto Board Virtual (XC4013E)
- J32 (XC4010)
- LCM (XC4005)
- LIRMM (XC4013E)
- Marc-1 (XC4005)
- MIT Nerd Kit (XCS30)
- MoM-3 (XC4000EX)
- MORRPH-ISA (XC4025)
- PCI Pamette V1 (XC4010E)
- PRISM-II (XC4010)
- P series Virtual Computer (XC4013E)
- R16 (XC4005)
- RISC4005 (XC4005)
- Rasa (XC4010)
- RC1000-II (XC4010E)
- RC1000-PP (XC40125XV)
- RPM (XC4013)
- SBX+ (XC4013E)
- SPARXIL (XC4010)
- Spectrum (XC4013)
- Spectrum2 (XC4020)
- SPLASH2 (XC4010)
- Spyder (XC4003)
- Spyder2 (XC4010)
- ST-FPGA (XC4xxx/XC5xxx)

**Xilinx XC6200 Series:**

- Hades (XC6216)
- RHO (XC6216)
- SPACE2 (XC6264)

**Xilinx XC9000 Series:**

- XS95 (XC9500)

**Custom IC:**

- Data-Flow Functional Computer
- DTM-1
- ProBoard
- TERAMAC

- perle-1 (XC3090)
- PRISM (XC3090)
- RENNS (XC3064)
- S56X2 (XC3064)
- SPLASH (XC3090)
- X-12 (XC3195)
- Zelig (XC3090)
- Tao (XC4013E)
- TbC-Pamette (XC4010)
- TM-1 (XC4010)
- V6502 (XC4013)
- VA1000 (XC4010)
- The Virtual Computer (XC4013)
- VZ80 (XC4013)
- XKL-1 (XC4013E)
- XS40 (XC4xxx/XC52xx)
- YARDS (XC4010)

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## Accelerator

**FPGA Devices:**
2 XILINX XC3195A
**On-board RAM:**
None
**External bus:**
OS Link 32 Way Din 41612 Socket, Mezzanine daughter-board connector.
**Interconnect:**
16 way configuration and 20 way data header, to daisy chain the boards.
**Contact:**
Embedded Solutions Ltd.
83 Gipsy Lane
Wokingham
Berks
RG40 2BW, UK
E-mail sales@nospam.embedded-solutions.ltd.uk
**Notes:**
The Accelerator is a supported target platform for the Handel-C V2.0 programming language. Unlike other programming languages, the output of this compiler is not a binary file; it is a net list. The Handel-C tools enable a software engineer to target directly FPGAs in a similar fashion to classical microprocessor cross-compiler development tools, without recourse to a Hardware Description Language. Thereby allowing the software engineer to realise directly the raw real-time processing capability of the FPGA. With Handel-C complete systems can be designed as a programming task, using only conventional and easily available programming skills. Source code and schematics are commercially available for the Accelerator to enable OEMs to rapidly produce custom variations of the design. More information is available at: http://www.embedded-solutions.ltd.uk

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## ACME

**FPGA Devices:**
14 Xilinx XC4010s and 6 Xilinx XC3195s
**On-board RAM:**
7 4K Dual-ported global memories each 4010 has a 4k Dual-ported memory
**External bus:**
SBUS
**Interconnect:**
The Adaptive Connectionist Model Emulator (ACME) is a Clos Network between 4010s and 3195s. The 3195s are used as programmable interconnect among 4010s and with global memory
**Contact:**
Pak K. Chan
Computer Engineering Board
225 Applied Sciences
University of California
Santa Cruz, CA 95064
Email: pak@nospam.cse.ucsc.edu
**Notes:**
See FPGA'94 Berkeley ACM Workshop

## Anyboard

**FPGA Devices:**
5 Xilinx 3042
**On-board RAM:**
384K
**External bus:**
ISA
**Interconnect:**
Fixed buses
**Contact:**
David E. Van den Bout
ECE Department
North Carolina State University
Raleigh, NC 27695-7911
**Notes:**

## APS X-84

**FPGA Devices:**
XILINX 4000 and 5000 84 pin PLCC family
**On-board RAM:**
None
**External bus:**
ISA
**Interconnect:**
None
**Contact:**
aaps@nospam.erols.com
**Notes:**
The APS X-84 is a low cost FPGA board which works with the XILINX 4000 and 5000 84 pin PLCC family of FPGA parts. The board allows the programming of parts from proms or PC ISA bus via supplied C code. On board oscillators and status LEDs are provided along with 24 bits of PC IO lines. The X-84 is a low cost PC ISA card with download software and sample VHDL and C code. It sells for $250.00.
See http://www.erols.com/aaps/ for more information.

## ARC-PCI

**FPGA Devices:**
3 FLEX EPF10K50
**On-board RAM:**
16MBytes
**External bus:**
PCI
**Interconnect:**
Fixed buses
**Contact:**
Stephen Smith
Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Tel: (408) 544-7666
E-mail: sjsmith@nospam.altera.com
WWW Page: http://www.altera.com/html/programs/phd.html
**Notes:**
One PLD comprises the system controller (PCI 32 bit initiator/target interface, on-board memory interface and user-configurable PLD configuration controller) and the other two are user-configurable PLDs. The memory hierarchy comprises one 1Mx32bits SRAM SIMM

cache per user-configurable PLD, and two independent 1Mx32bits SRAM SIMM memories which all three PLDs directly access. The cache signals of each user-configurable PLD also drive external I/O which may be used to access external memory. These platforms are available for free to qualified researchers.

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## ArMen

**FPGA Devices:**
1 3090 per node. The MIMD/FPGA parallel machine is modular and extensible.
**On-board RAM:**
1, 2 or 4Mb/node each board has a T805 processor with 4 20Mb/s links.
**External bus:**
SBUS Archipel board with a T805. I/Os can be handled directly within ArMen using additional transputer/peripheral boards.
**Interconnect:**
Processor interconnection is host system dependent. We have two 8 nodes computers configures as cubes. 3090 south and west ports are assembled into a linear ring with 36bits data path. North ports are mapped in the processor address space, so that they receive address/data from their local processor. The FPGA 32 bit south port is free for extensions or input/output on each node.
**Contact:**
Bernard Pottier
Laboratoire d'Informatique de Brest
Universite de Bretagne Occidentale
UFR Sciences, BP 802,
Brest, 29285, FRANCE.
Email: pottier@nospam.univ-brest.fr
**Notes:**
See Napa FCCM 93 and 94 or Hawai HICSS-94 proceedings. ArMen can easily be connected to any host having an interface board for transputers. There are projects for commercial distribution.
More information is available at: http://ubolib.univ-brest.fr/~armen/armen1-eng.html.

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## BORG

**FPGA Devices:**
2 Xilinx 3030s and 2 Xilinx 3042s
**On-board RAM:**
2K
**External bus:**
PC-bus interface in 5th FPGA
**Interconnect:**
4 FPGAs in a Clos network 2 FPGAs can be used as interconnect or logic
**Contact:**
Pak K. Chan
Computer Engineering Board
225 Applied Sciences
University of California
Santa Cruz, CA 95064
Email: pak@nospam.cse.ucsc.edu
**Notes:**
25 boards made by Xilinx and distributed for educational purposes. See FPGA'92 Berkeley ACM Workshop

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## BORG-II

**FPGA Devices:**
2 Xilinx 4003As and 2 Xilinx 4002As
**On-board RAM:**
8K

**External bus:**
PC-bus interface in 5th FPGA
**Interconnect:**
4 FPGAs in a Clos network 2 FPGAs can be used as interconnect or logic
**Contact:**
Pak K. Chan
Computer Engineering Board
225 Applied Sciences
University of California
Santa Cruz, CA 95064
Email: pak@nospam.cse.ucsc.edu
**Notes:**
100 boards made by Xilinx and distributed for educational purposes. FPGAs are socketed and can be replaced by any 4000 series pc84 part.

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## Chameleon

**FPGA Devices:**
7 Algotronix CAL
**External bus:**
**Interconnect:**
Fixed mesh
**Contact:**
Cuno Pfister
pfister@nospam.oberon.ch
**Notes:**
Experimental workstation from ETH Zurich with FPGA's closely coupled to MIPS R3000 processor and innovative object based design software written in the Oberon language.

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## CHAMP

**FPGA Devices:**
16 Xilinx 4013
**On-board RAM:**
512K Dual-ported
**External bus:**
VME
**Interconnect:**
Crossbar (using FPGAs)
**Contact:**
Brian Box
Lockheed Sanders
NCA01-2244
P.O Box 868
Nashua, NH 03060
Phone: (603) 885-7487
FAX: (603) 885-9056
Email: box@nospam.nhqvax.sanders.lockheed.com
**Notes:**
The Configurable Hardware Algorithm Mappable Processor (CHAMP) is used primarily for hardware prototyping.

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## Cheops

**FPGA Devices:**
ORCA
**On-board RAM:**
3 MB
**External bus:**
???

**Interconnect:**
???
**Contact:**
???
**Notes:**
The Cheops Imaging System is a compact, modular platform for acquisition, real-time processing, and display of digital video sequences and model-based representations of moving scenes. It is a laboratory tool and a prototype hardware and software architecture for future programmable video processors. Cheops abstracts out a set of basic, computationally intensive stream operations that may be performed in parallel and embodies them in specialized hardware. In order to simplify programming, a resource management daemon handles the real-time scheduling and allocation.
See: http://cheops.www.media.mit.edu/projects/cheops/ for more information.

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## CHS 2x4

**FPGA Devices:**
9 Algotronix CALs (1 controller + 8 compute)
**On-board RAM:**
2 MB SRAM
**External bus:**
ISA
**Interconnect:**
Fixed mesh
**Contact:**
Tom Kean
Xilinx Development Corp.
53 Mortonhall Gate
Edinburgh EH16 6TJ
Phone: 44 31 666 2600ext204
Fax: 44 31 666 0222
Email: tomk@nospam.xilinx.com
**Notes:**
Based on work at the University of Edinburgh by Tom Kean and John Gray. Commercialized by Algotronix. Algotronix purchased by Xilinx in 1993. System cascadable to 2 boards. No longer commercially available.

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## Data-Flow Functional Computer (DFFC)

**Application area:**
Real-Time Image Processing
**FPGA Devices:**
512 custom-built Field-Programmable Operator Arrays (FPOA). Each FPOA contains 2 Configurable Data-Paths (8/16 bit operators) and 10 I/O Ports (10-bit bidirectional bus interface).
**On-board RAM:**
Each Configurable Data-Path includes a 256x9 RAM that can be used as a FIFO, as a dual port RAM operator or as local RAM for specific purposes (histogrammer). Additionnaly, two 4MByte RAM boards are currently connected to the DFFC.
**External bus:**
VME (Sun SPARC2 as host)
**Interconnect:**
The DFFC is a 3D 8x8x8 array of FPOAs, resulting in a 16x8x8 array of Configurable Data-Paths (CDP). Each CDP has direct access to its 6 neighbors (local connections). Long distance connections are possible through Configurable Data-Paths and I/O Ports configured as routing elements.
**Contact:**
Georges M. Quenot
LIMSI-CNRS,
BP133, 91403 Orsay Cedex FRANCE
Email: quenot@nospam.limsi.fr / quenot@nospam.etca.fr
or

Ivan C. Kraljic
Laboratoire Systeme de Perception
DGA/Etablissement Technique Central de l'Armement
16 bis avenue Prieur de la Cote d'Or,
94114 ARCUEIL Cedex FRANCE
Email: ik@nospam.etca.fr

**Notes:**

See: `A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping', IEEE Workshop on FPGAs for Custom Computing Machines, 1994, pp 91-100. Available at http://www.etca.fr/Articles/Theme2/Kraljic/

The Data-Flow Functional Computer is dedicated to rapid prototyping of real-time vision automata. The Computer consists of a regular 3D array of very coarse grain application-specific FPGA called the Field-Programmable Operator Array (FPOA).The FPOA granularity is at the 8/16 bit operator level instead of at the gate level. Its architecture has been designed to implement efficiently a wide range of low-level image processing basic operators Specific development tools allow an easy and efficient use of the Computer: a high-level description (in a functional language) is compiled into a DFFC configuration using an Operator Library. An environment for automatic derivation of vision automata from a DFFC configuration is currently under development.

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## CM-2X

**FPGA Devices:**

16 Xilinx 4005

**On-board RAM:**

None

**External bus:**

Fixed

**Interconnect:**

None

**Contact:**

Craig Reese
IDA Supercomputing Research Center
17100 Science Drive
Bowie, MD 20715
Phone: (301) 805-7479
FAX: (301) 805-7602
Phone: cfreese@nospam.super.org

**Notes:**

A Connection Machine 2 SIMD machine from Thinking Machines Corporation with the Weitek WTL3164 floating point processors replaced by Xilinx 4005s. De-commissioned 1994.

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## 9204/FPGA/DS-link

**FPGA Devices:**

Two Xilinx XC4025E2HQ240C or XC4028EX2HQ240C devices.

**On-board RAM:**

32kx16 of 12ns SRAM per Xilinx device, plus shared access to the communications processor and its 8MB of DRAM.

**External bus:**

Four IEEE 1355 100Mb/s DS Links, Size 4 HTRAM module format.
For use in any IEEE 1355 DS-Link based HTRAM system such as the Parsys SN9000 series or VITA 13-1995 based VME systems.

**Interconnect:**

Four IEEE 1355 100Mbit/s DS Links via T9000 communications processor.
Two 50 pin headers providing direct access to 25 Xilinx pins per Xilinx device, suitable for interfacing to external signal sources and output devices.
Internal 65 bit bus connecting the two Xilinx devices together independently of the other interfaces.

**Contact:**

Parsys Ltd.

Boundary House
Boston Road
London W7 2QE
UK
Tel: +44 181 579 8683
Fax: +44 181 579 8365
E-mail info@nospam.parsys.co.uk

**Notes:**

The 9204/FPGA is a reconfigurable FPGA based module designed for use within IEEE 1355 DS-Link based systems and VITA 13-1995 VME systems. Each module contains two Xilinx 240 pin XC4025E or XC4028EX devices and a T9000 communications processor allowing communication via four 100 Mbit/second DS links between the Xilinx devices and the rest of the multiprocessor system. Dual programmable frequency synthesisers are provided for frequency generation up to 100MHz. Each Xilinx device may be configured using standard development tools to provide user defined processing functions, with macro libraries supplied for message passing across the DS link network and for access to the local SRAM and shared DRAM memory. Each Xilinx may be configured and reconfigured under program control by the communications processor using a fast download of bit-mapped configuration files.

Powerful embedded systems can be constructed using any mix of reconfigurable FPGA nodes, processing nodes and I/O nodes to suit the requirements of an application, with fast efficient message passing available between all nodes. Interfaces are also available to connect the systems to standard PCs and Unix workstations. More information is available from http://www.parsys.com/

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## DSP-56X

**FPGA Devices:**

1 Xilinx 3042

**On-board RAM:**

32KW-128KW (shared with DSP56000)

**External bus:**

SBus & Flexible

**Interconnect:**

See notes below.

**Contact:**

Michael C. Peck
President
Berkeley Camera Engineering
3616 Skyline Drive
Hayward, CA 94542-2521
Phone: 510-889-6960
Fax: 510-889-7606
email: mikep@nospam.bce.com

**Notes:**

The DSP-56X is an SBus card that contains a 40MHz Motorola 5600x family DSP, a Xilinx 3042, and memory (32K words or 128K words I believe). The 3042 sits directly on the 56000 bus and can be accessed from either the 56000 or the SBus. Some of the Xilinx pins are connected to the SBus back panel connector.

See S56X2.

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## DTM-1

**FPGA Devices:**

16 DTM chips

**On-Board RAM:**

32 8K x16 SRAM banks on separate DTM ports, dual ported to host

**External bus:**

VME

**Interconnect:**

Packed Exponential Connections (a multi-grid mesh network)

**Contact:**

Worth Kirkman
MITRE Corporation
7525 Colshire Dr.
McLean, VA 22102
Phone: (703)883-7082
FAX: (703)883-6708
Email: kirkman@nospam.mitre.org

**Notes:**

Built from custom DTM chips. These devices are custom RAM-configurable 64x64 arrays of expandable-gate cells, each pipelined for 2 boolean input evaluations in a 100MHz cycle. 256 I/O pins, each arbitrary direction with echo-cancellation and programmable parallel<=> serial sub-sampling - normally run at 1/4 the internal rate.

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## DVC1 - Distributed Virtual Computer

**FPGA Devices:**

2 - Xilinx XC-4013E-3 FPGA

**On-board RAM:**

1MEG SRAM

**External bus:**

Single Slot SBus Board for SUN Compatible Workstations

**Interface:**

The interface between the your design and the host workstation is handled by the use of a VCC SBus interface Macro placed into the design. Interface Macros (schematic, Verilog & VHDL), 'C' Programming Language function routines and Conversion Program for implementing designs from with a 'C' Program Application are available with the SBus Software Interface Kit.

Two SBus Interface Kits are available: Slave Interface Kit and Master Interface Kit. (Design Entry & Implementation Software is needed).

For more information on **Hardware Object Technology** Programming see: VCC's HOT Programming

**Specifications:**

On-Chip Clock & Data Recovery PLL
32 bit CRC & Parity Generate/Check
8b/10b Encode/Decode of data, ordered sets and line states
Compliance to Fibre Channel Specs of Accredited Standards Committee (ACSX3T9.3)
1 Megabytes SRAM (256Kx32bit 20ns Access Time)
4 Kbytes FIFOs for transmit and receive data
SMA Coax Connectors (50 Ohm)
Programmable Oscillator (360KHz to 120MHz)

**Contact:**

John Schewel
Virtual Computer Corporation
6925 Canby Ave #103
Reseda CA 91335 USA
Email: jas@nospam.vcc.com
Tel: (818) 342-8294 Fax: (818) 342-0240
Visit Our Web Site at: VCC's Home Page

**Notes:**

The **Distributed Virtual Computer$^{tm}$ (DVC)**, reconfigurable computer is an extension of the EVC1 product line. These add-on modules allows one to connect multiple EVC1 systems in a true compute through independent virtual network on existing SUN workstations. Each EVC1/DVC1 combination is a user customizable computing node with the ability to be used independently of the host system. The DVC1 The Virtual Computer Net$^{tm}$ allows data to be processed as it passes over the net, independent of the host; yet each node has the entire resources of the host if needed. VCC's software driver, bus interface, Hardware Object Macros and functions gives the designer the ability to create multiple communication protocol designs. Dynamic re-programmablity allows the network to change communication protocols on the fly, node by node. The reconfigurable aspect of each node can allow different communications protocols to be used within the same network pathway. In a clustered workstation environment the compute through Virtual Computer Net can be used for high performance computing applications.

More information on the DVC1 is available at: VCC's Website for DVC1.

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## EDgAR-2

**FPGA Devices:**
4 Xilinx XC4013XLT
**On-board RAM:**
None
**External bus:**
PCI
**Interconnect:**
Two 40-pins headers, one 72-pins header, a 32-bits path between each FPGAs pair (building a chain), a 4-bits path between each CPLDs pair (building a chain), an 8-bits connection between each CPLD-FPGA pair
**Contact:**
Antonio J A Esteves
Informatics Department, University of Minho
Largo do Paco
4709 Braga Codex, Portugal
Email: esteves@nospam.di.uminho.pt
**Notes:**
The EDgAR-2 is a standard PCI bus card suitable to deal with the hardware/software codesign paradigm. The architecture is based on FPGA-CPLD pairs, supporting computional models like FSMD (FSM with datapath), CFSMD (concurrent FSMD) or PSM (program state machine). The CPLDs included on the board are Xilinx XC95108. The two 40-pins headers can be used to build a daisy-chain of boards.
The support software provides NT.4.0 driver for the board.

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## ENABLE++

ENABLE++ is a modular FPGA multiprocessor system and contains three kinds of boards. For a description see below.

## Matrixboards

**FPGA Devices:**
Sixteen Xilinx XC4013 (core), 11 Xilinx XC5005H, eight of them used as backplane interface and three for control.
**On-board RAM:**
12MB SSRAM (synchronous SRAM) configured as 48 banks of 128K*18 (20ns), eight banks of 4K*18 (20ns) synchronous dual ported RAM.
**External Bus:**
Four Transputer Links on LCM (see below).
Eight 32bit ports (200 MByte/s) to Backplane.
**Interconnect:**
Eight I-Cube I240 FPIDs for global interconnections between 16 core FPGAs and eight IO-FPGAs, 40 bit wide busses (250MByte/s).

## IO-Boards

**FPGA Devices:**
Eighteen Xilinx XC4005H, seven used as module controllers, eight as backplane interface and three for control.
**On-board RAM:**
Eight banks of 4K*18 (20ns) and seven banks of 4K*36 (20ns) synchronous dual ported RAM.
IO-Board modules with 128MB DRAM, 32 bit wide, 200MByte/s, up to three modules (384MB) can be plugged on one IO-Board.
**External Bus:**
Four Transputer Links on LCM (see below).
Eight 32 bit wide ports (200MByte/s) to Backplane.

IO-Modules for different busses (planned): Hippi, Hot-Link, Fiber Channel, DS-Link.

**Interconnect:**

Four I-Cube I240 FPIDs for global interconnections between seven module slots, one LCM slot and eight IO-FPGAs, 32 bit wide busses (200MByte/s).

## Backplane

**FPGA Devices:**

Four (optional eight) Xilinx XC4005H for each of up to six slots.

**On-board RAM:**

None

**External Bus:**

Four Transputer Links on LCM (see below) and
up to six slots with eight 32 bit wide ports (200MByte/s).

**Interconnect:**

Interconnections (40 bit) between neighbouring FPGAs which control corresponding ports of different slots.

**Contact:**

K.H. Noffz
Lehrstuhl fuer Informatik V
Universitaet Mannheim
Seminargebaude A5
68131 Mannheim (Germany)
Phone: 49-621-292-5755
Fax: 49-621-292-5756
e-mail: noffz@nospam.mp-sun1.informatik.uni-mannheim.de

**Notes:**

Enable++ is a scalable general purpose FPGA multiprocessor system. It contains a single reconfigurable Backplane which connects up to six Matrix- and IO-Boards. FPGAs for computation are located on the Matrix-Boards (core) while up to seven modules with different kinds of interfaces and custom hardware (DSP's, uP's, RAM, ...) can be plugged on IO-Boards. Therefore the system can be easily expanded with custom hardware for special purposes.

Every Backplane-, Matrix- and IO-Board is controlled by an LCM (Local Control Module) which contains a single Transputer (T425 or T800) and one Xilinx XC4005. LCMs use Transputer Links to communicate with the host Workstation.

Software:

SPC-Compiler (Systolic Parallel C), Simulator, Realtimedebugger (handles SPC sourcecode), VHDL-Compiler.

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## epX31

**FPGA Devices:**

1 ALTERA EPX780 in 84-pin PLCC

**On-board RAM:**

32 KByte

**External bus:**

IBM-PC printer port

**Interconnect:**

None

**Contact:**

XESS Corp.
1-800-549-XESS
1-919-387-0076
fpga-info@nospam.xess.com

**Notes:**

The epX31 is a small 4"x 2" board containing an ALTERA EPX780 FPGA in 84-pin PLCC package, an 8031 microcontroller, and a 32 KByte RAM. The epX31 FPGA is programmed using the PLDasm HDL and Intel's free PLDshell Plus programming environment. The 8031 is programmed using MetaLink's 8051 cross-assembler or any other assembler or compiler that outputs a standard .HEX object file. FPGA configuration files are downloaded to the epX31 through the PC printer port using the JTAG protocol. 8031 object code is also loaded into the 32 KByte RAM through the printer port. The FPGA is treated as a

reconfigurable peripheral of the 8031. Additional signals from the printer port can be used to exercise the downloaded design. The results can be observed using the 7-segment LED on the epX31 or sent back for display on the PC. The epX31 can be used stand-alone or it can be mounted in a breadboard (all the pins for the FPGA, microcontroller and RAM are made available on two rows of 42 pins each). Since configuration is done using a JTAG stream, it is easy to cascade multiple epX31s to experiment with multiprocessor and multi-FPGA systems.

A book accompanies the epX31:

"FPGA Workout". Softcover, 240 pp., 120 illustrations, and index. ISBN 0-9642187-0-4.

This book shows how to use FPGAs to build digital systems ranging from simple combinational logic up to a 4-bit microcontroller. All PLDasm examples in the book can be downloaded into the epX31 and tested. A separate addendum is included showing how the 8031 can use the FPGA as a reconfigurable memory-mapped device.

The epX31 has been replaced by newer hardware. See the XESS web site for further information.

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## EVC

**FPGA Devices:**

1 Xilinx 4010

**On-board RAM:**

Daughter board (see notes)

**External bus:**

SBus

**Interconnect:**

None

**Contact:**

Steve Casselman
Virtual Computer Corporation
Reseda, CA 91335
Phone: (818) 342-8294
FAX: (818) 342-0240
Email: sc@nospam.vcc.com

**Notes:**

The Engineers Virtual Computer (EVC) is a single FPGA based transformable computing system. It has a daughter board area that has 96 user I/O from the 4010. A 2 Meg fast SRAM daughter board is available now.

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## EVC1 -- Virtual Computer

**FPGA Devices:**

1 - Xilinx XC-4013E-3 FPGA

**On-board RAM:**

2MEG SRAM Daughter Board (Optional)

**External bus:**

Single Slot Sbus Plugin Board for SUN Compatible Workstations

**Interface:**

The interface between the your design and the host workstation is handled by the use of a VCC SBus interface Macro placed into the design. Interface Macros (schematic, Verilog & VHDL), 'C' Programming Language function routines and Conversion Program for implementing designs from with a 'C' Program Application are available with the SBus Software Interface Kit.

Two SBus Interface Kits are available: Slave Interface Kit and Master Interface Kit. (Design Entry & Implementation Software is needed).

For more information on **Hardware Object Technology** Programming see: VCC's HOT Programming

**Other Options:**

A Programmable Oscillator Module is available. This module plugs into a socket on the EVC1 and is programmable via a POM Macro from 360 KHz to 120 MHz.

**Contact:**

John Schewel
Virtual Computer Corporation

6925 Canby Ave #103
Reseda CA 91335 USA
Email: jas@nospam.vcc.com
Tel: (818) 342-8294 Fax: (818) 342-0240
Visit Our Web Site at: VCC's Home Page

**Notes:**

The **EVC1 Virtual Computer[tm]**, reconfigurable computer is a single SBus board based reconfigurable computing system utilizing Field Programmable Gate Array (FPGA) technology. The user can create a a personal coprocessor, customized to their specific computing needs. The EVC1 allows the developer to craft a custom hardware solution for software application acceleration. You can create hundreds of special purpose coprocessing chips, downloading them in sequence using a program. The EVC1 also serves as an Emulation and/or Rapid Product Development System. The EVC1 can be reconfigured in 150 milliseconds.

The EVC1 has been designed for maximum flexibilty through the 96 Bits of User I/O to a Daughter Board area. The capabilities of the EVC1 are extended through the use of various standard Daughter Boards, such as the 2Meg SRAM module and communications module. Complete schematics are supplied for integrating user-made custom Daughter Board Modules.
More information on the EVC1 is available at: VCC's Website for EVC1.

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## The Flexible Processor

**FPGA Devices:**

8 Xilinx XC3020

**On-board RAM:**

64KB Data + 256KB Microprogram

**External bus:**

RS232 via MC68HC11 System Controller

**Interconnect:**

Fixed - Several topologies

**Contact:**

Andrew Wolfe
Dept. of Electrical Engineering
Princeton University
Princeton, NJ 10544
awolfe@nospam.princeton.edu

**Notes:**

Also includes hardwired FP unit. Built in '87-'88 as a technology demonstration at Carnegie Mellon - long since decomissioned. Published description at Micro 21 - 1988.

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## Functional Memory Computer

**FPGA Devices:**

Up to 8 Xilinx XC4010s plus 3 Xilinx XC4013s

**On-board RAM:**

1 MB SRAM configured as 1 bank of 128K by 32 bit data RAM and 1 bank of 128K by 32 bit microprogram RAM. Can be configured as 1 bank of 128K by 64 bit of data RAM.

**External bus:**

PCI short and long card versions

**Interconnect:**

Up to 12 FPGAs are memory mapped on a 32-bit bus with the 13th FPGA configured as a microprogrammable processor. An additional single bit daisy chain links 8 XC4010s. 74 bits interconnect two XC4013s.

**Contact:**

Richard Halverson, Jr.
Information and Computer Sciences Dept.
2565 The Mall, Keller Hall 319
University of Hawaii at Manoa
Honolulu, HI 96822
Email: richardh@nospam.hawaii.edu, http://www.ics.hawaii.edu/~richardh/

**Notes:**

More information on functional memory is available. The project is supported by the Office of Technology Transfer and Economic Development at the University of Hawaii at Manoa.

## G-800

**FPGA Devices:**

Grouped in modules (maximum 16 -- see Notes below)

**On-board RAM:**

See Notes below

**External bus:**

VESA (VL) Local bus VESA Media Channel - 100 MB/sec video bus 80 pin connector supports 32 bit devices

**Interconnect:**

Bus Oriented Communication - Virtual Bus All Interconnect via Xilinx 4010's on G-800 2x32 bit buses and 2x16 bit buses on G-800 Configuration is programmable - Virtual Bus

**Contact:**

bovarga@nospam.gigaops.com
2374 Eunice St.
Berkeley, CA. 94708

**Notes:**

Modules have standard form factor and pinout. All bus lines to G-800 connect via FPGAs. Up to 16 modules of all types on 1 G-800 board.
Visual Computing Module (VMC)= 2xXC4005; 4MB DRAM and 80 MIPS DSPS
PGA10MOD = 1 x XC4010, 2MB DRAM, 128K SRAM PROTOMOD = same as PGA10MOD with pinouts extended to pads for wirewrap, logic analyzer, etc.
16xVCMs = 32 XC4005's, 2 XC4010's on G-800, 64 MB DRAM 16xPGA10MODs = 16 XC4010's, 2 XC4010's on G-800, and 32 MB DRAM and 2 MB SRAM
XPGAMOD = 4xXC4010, 8 MB DRAM, 512K SRAM (available Oct) 16xXPGAMODs = 32 XC4010's, 2 XC4010's on G-800, and 128 MB DRAM and 8 MB SRAM

## G-900 RIC

**FPGA Devices:**

2 XC-PQ240 FPGAs on Reconfigurable Interface Card (9800-RIC). Normally XC4013E + XC5210-5. However, XC4010E, XC4013E, XC4020E, XC4028EX can be substituted for the XC5210-5. The G900 is socketed for 16 XMODs™

**On-board Memory:**

512KB surface mounted Flash, 128KB socketed Flash, 128KB SRAM

**External busses:**

Eight 32-bit busses - maximum 128-bit I/O @ 33MHz to 80MHz.
Four 34-bit I/O ports via 68-pin edge fingers.
Four 36-bit I/O ports via 50-pin male IDC connectors.
Application specific I/O is provided via I/OMODS™ (see SPECTRUM2).

**Interconnect:**

130-pin Virtual Bus Architecture programmable for 32-bit pipelines, global busses, isolated busses, rings, meshes, etc.
All interconnect is via Xilinx FPGAs on G900 RIC and is programmable.
Dataflow specific bandwidths vary from 96-bit global busses @ 20 MHz to 32-bit pipelines @ 76 MHz.

**Clocks:**

8 low skew clocks are provided per XMOD, 5 per FPGA. These can be internal, external, self clocking data streams, PLLs, FGENS, XTALs, etc.

**Contact:**

bo@nospam.gigaops.com
2510 MLK Way
Berkeley, CA 94704
Phone (510) 848-5446
Fax (510) 848-5667
WWW: http://www.reconfig.com, click on Sponsors, then Giga Ops logo.

**Notes:**

G900 is socketed for 16 XMODs or I/OMODs as 4 stacks of 4 each. XMODs have 2

XC4000 series PQ208 FPGAs on a 2.4" x 3.65" card with 2 100-pin stacking connectors on the top and bottom. 16 XMODs deliver 32 FPGAs, 128MB DRAM, and 4MB SRAM.
XMODs may also be used as embedded processors. Contact docmgr@nospam.gigaops.com for the XMOD Design Specification.
See SPECTRUM2 LISTING for more details.

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## GANGLION

**FPGA Devices:**
24 Xilinx 3090
**On-board RAM:**
24K PROM
**External bus:**
VME / Datacube MAXbus
**Interconnect:**
Fixed
**Contact:**
Charles Cox
IBM Research Division
Almaden Research Center
San Jose, CA 95120-6099
**Notes:**
Used exclusively for neural networks.

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## Hades, ETH Zurich

**FPGA Devices:**
1 Xilinx XC6216
**On-board RAM:**
256 KB static RAM
**External bus:**
Ceres-Bus (ETH proprietary)
**Interconnect:**
**Contact:**
Stefan H.-M. Ludwig
Institute for Computer Systems (RZ H3)
Swiss Federal Institute of Technology
ETH Zentrum
CH-8032 Zurich
Email: ludwig@nospam.inf.ethz.ch

**Notes:**
Hades: Integrating hardware and software
We develop a hardware description system for Field-Programmable Gate Arrays (FPGAs). On the hardware side of our project, a XC6200 FPGA is used as a universal co-processor in a computer system. On the software side, fast physical design algorithms are used for efficient, automatic hardware development, where the user can influence the design process at several stages. Furthermore, we try to close the semantic gap between hardware and software using a novel approach to combining the description of hardware and software with the help of a type-safe interface between the two components.
See also FPL'96 Darmstadt.

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## HARP1

**FPGA Devices:**
1 Xilinx 3195
**On-board RAM:**
64K SRAM / 4MB DRAM
**External bus:**
4 x 20Mbit/sec transputer links + expansion port (spare FPGA pins)

**Interconnect:**
FPGA shares RISC processor bus
**Contact:**
Ian Page
Oxford University Computing Laboratory
Wolfson Building, Parks Road, Oxford OX1 3QD, U.K.
Phone: +44 1865 273853
FAX: +44 1865 273839
EMail : Ian.Page@nospam.comlab.ox.ac.uk
**Notes:**
The HARP1 is an industry standard TRAM board (size 6 = 165 x 84mm) containing a 32-bit RISC-style microprocessor (a T805 transputer) with 4 Mbytes of dynamic RAM. Two independent banks of 32K x 16-bit fast static RAM are attached to the Xilinx 3195 Field Programmable Gate Array. The FPGA has full access to the microprocessor bus. A 100MHz frequency synthesiser is used for arbitrary clock generation. An expansion port is connected to the spare FPGA pins. TRAM motherboards allow for easy integration into a variety of host systems, or for connecting multiple HARP boards together.
This board will be commercially available around 2Q95 from:
Sundance Multiprocessor Technology Ltd.
4 Market Square
Amersham, Bucks HP7 0DQ, U.K.
+44 494 431203 (fax 726363)
For more information see: Ian Page's Homepage or The HARP Boards.

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## ipEngine-1

**FPGA Devices:**
1 EPF6016
**On-board RAM:**
128Kx18 Sync SRAM
**External bus:**
None - Board contains PowerPC CPU, 16 MB DRAM, 2 MB FLASH
**Interconnect:**
Dual 66x2 Headers with a total of 88 pins of virtual I/O
**Contact:**
Bright Star Engineering Inc.
19 Enfield Drive
Andover MA 01810 USA
Tel: +1-978-470-8738
Fax: +1-978-470-8878
Email: sja@brightstareng.com
Web: http://www.brightstareng.com/
**Notes:**
The ipEngine-1 contains the following features:
16,000 Gate FPGA
PowerPC RISC CPU
16 MB DRAM
2 MB Flash
On-Board Power Supply
Ethernet
USB and Serial Ports
LCD/TV Video
Integrated RTOS and Web Server

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## Virtual *ISA* Proto Board -- Virtual Computer

**FPGA Devices:**
1 - Xilinx XC-5210-6 FPGA OR Xilinx XC-4013E-3 FPGA
**On-board RAM:**
Support for 2 - 30pin SIMMs (SIMMS not included), EPROM and 32KB SRAM
**External bus:**
Single Slot ISA Bus Plugin Board for IBM Compatible Computers

**Specifications:**

Supports 8/16 bits ISA operation mode, Plug n Play spec.V1.0a and Windows 95 ready
Fujitsu MB86701 Plug and Play interface for fully compliant interface (includes all drivers & config.)
Two user feed through grids areas (opposite ends of board), for Analog and Digital prototyping
Ground and power test points --- Separate power and ground planes for signal integrity (TBD)
All Xilinx pins available on .100=F6 headers --- Silk screen coordinates and Signal list for ease of use
Xilinx FPGA supports all configuration modes: including, Serial Slave (Xchecker), Master Parallel (on board ROM), Master Serial (on board serial ROM) or from host bus
Logic Analyzer interface for industry standard HP logic analyzer through auxillary connect board

**Other Options:**

A Programmable Oscillator is available. This module plugs into a socket on the ISA Board and is programmable via a POM Macro from 360KHz to 120 MHz.
A Multi-FPGA Daughter Board is available. This module plugs into the breakout pins of the Proto Board's FPGA. The Multi-FPGA Daughter Board comes in two configurations: 4- Xilinx XC-5210-6 OR 4- Xilinx XC4013E-3.

**Contact:**

John Schewel
Virtual Computer Corporation
6925 Canby Ave #103
Reseda CA 91335 USA
Email: jas@nospam.vcc.com
Tel: (818) 342-8294 Fax: (818) 342-0240
Visit Our Web Site at: VCC's Home Page

**Notes:**

The **Virtual ISA Proto Board**[tm] , is a reconfigurable development system with prototyping features. It provides an integrated tool set consisting of software driver, Windows software support, Plug n Play interface, and a reference logic configuration library for canned configurations for the on-board FPGA.
Hardware features of the standard board include 10,000 to 13,000 reconfigurable logic gates, signal break-outs, logic analyzer interface, a Plug n Play interface, two PCB grid areas, and an optional programmable oscillator. All Xilinx pins broken out for ease of logic analysis. The - Virtual ISA Proto Board provides a low-risk platform for the immediate trial and implementation of new projects and continuing development.
More information on the ISA Proto Board is available at: VCC's Website for the Virtual ISA Proto Board.

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## J32

**FPGA Devices:**

1 Xilinx XC4010-5

**On-board RAM:**

1Mx32 70 ns FPM DRAM SIMM

**External bus:**

RS-232 and DRAM interface

**Interconnect:**

none

**Contact:**

Jan Gray
(computer architecture hobbyist)
Redmond, WA
(206) 881-7567
Email: jsgray@nospam.ix.netcom.com

**Notes:**

Architecture: 32-bit RISC. 32x32 register file. 3 operand instructions: "d = s1 op s2" or "d = s1 op immed" including add/sub, and/or/xor/xnor, 1- and 2-bit shifts and rotates. Load/store signed/unsigned byte, halfword, word, using "reg + immed" effective address. Z,N,C,V condition codes altered on most operations. 2-cycle delayed branch conditional jumps and subroutine call (jump and link).
Implementation: 20x11 CLBs. 16 MIPS, clocked at 33 MHz. Traditional IF/RF/EX/WB

pipeline. Load/store stalls pipeline. On-chip DRAM control, RS-232 interface, boot ROM. Design specified in C++ based circuit specification language. Currently only programmed in assembler.

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## LCM

**FPGA Devices:**
One Xilinx X4005 (PG156)
**On-board RAM:**
4-32MB DRAM.
**External Bus:**
Four Transputer-Links, one 32 bit wide LCM port (45 bit including control lines, clocks and IRQ lines).
**Interconnect:**
FPGA shares RISC CPU bus.
**Contact:**
A. Kugel
Lehrstuhl fuer Informatik V
Universitaet Mannheim (Germany)
Seminargebaeude A5
68131 Mannheim
Phone: 49-621-292-5755
Fax: 49-621-292-5756
e-mail: kugel@nospam.mp-sun1.informatik.uni-mannheim.de
**Notes:**
LCM stands for Local Controller Module. It is a small Transputer module (PCB 85x135mm, equiped with a T425 or T800 Transputer) with additional FPGA hardware. Once booted by a host Workstation via one of its Transputer Links it configures and controls the Backplane, Matrix- and IO-Boards of the ENABLE++ system. It is a crucial component for debugging SPC programs on the Enable hardware but can be used standalone as well.
Software: C-Compiler, Debugger, VHDL sample code for mapping CPU bus to external port.

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## LIRMM

**FPGA Devices:**
2 Xilinx XC4013Es
**On-board RAM:**
2 x 1 Mbit
**External bus:**
ISA or S-bus
**Interconnect:**
Connected to TMS320C40 DSP
**Contact:**
L.TORRES (Phd student) or
M.ROBERT (Professor), or
G.CAMBON (LIRMM director)
University of Montpellier II
LIRMM
(Laboratory of Informatic, Robotic and Microelectronic of Montpellier)
161 Rue ADA
34 392 Montpellier Cedex 5
FRANCE
E-mail : {torres},{cambon},{robert}@nospam.lirmm.fr
Phone : (33) 67-41-85-85
FAX : (33) 67-41-85-00
**Notes:**
LIRMM stands for Logic Inside Reconfigurabe Micro Machine. The LIRMM approach is to develop a hardware/software prototyping system based on the combination of FPGA Xilinx and DSP TMS320C40 chips; the main features of the prototyping system are :
-flexible interfaces with the designer;
-flexible implementation due to use of Field Programmable Gate Arrays;

-PC or UNIX based software to configure and control the board:
-interface with common commercial board (Hunt Engineering, TIM40 format).
We have realized a protocol communication with the DSP chip. The result obtained, with a 40 Mhz clock rate, is a communication transfer data between DSP and Xilinx at 16 Mbytes/s.
Presently, 7 boards are built and they will be used for:
- research: experimentation of the HW/SW design methodology under development;
- education on HW/SW system design.
These boards a hosted by :
- PC/ DOS;
- UNIX (4 boards connected to a SPAC20 workstation).
You can find more details in our Web page : http://www.lirmm.fr/~maillet/CoDesign/

## Marc-1

**FPGA Devices:**
25 Xilinx 4005 (18 processing + 5 interconnect + 2 control)
**On-board RAM:**
6 MB
**External bus:**
SBus
**Interconnect:**
5 Xilinx 4005
**Contact:**
David M. Lewis
University of Toronto
Department of Electrical Engineering
Toronto, Canada
Email: lewis@nospam.eecg.toronto.edu
**Notes:**
Marc-1 consists of two modules. Each module contains an instructions unit of 3 Xilinx 4005s, a datapath of 6 Xilinx 4005s, a 256K x 64 instruction memory, a 256K x 32 data memory and a Weitek 3364. These are connected by an interconnect module of 5 Xilinx 4005s. Two more Xilinx 4005s are used to interface to the Sun Sparc host.

## MIT Nerd Kit

**FPGA Devices:**
Xilinx 4000XL in base, 16 XCS30 spartans in device array
**On-board RAM:**
2 MB DRAM
**External bus:**
IEEE1284 plus RS232 for config info only
**Interconnect:**
User-Configurable Serialized Wires
**Contact:**
bunnie@nospam.mit.edu
**Notes:**
The MIT Nerd Kit is the affectionate moniker given to the lab kit that undergraduate EECS students use to build devices ranging from simple FSMs to multiprocessor computer systems based on simple 32-bit RISC microprocessors. The lab kit features a device array of 16 FPGAs that can be configured to emulate compution structures ranging from simple boolean functions to 32-bit RISC microprocessors. Students connect computational blocks using wires that carry data in a 32-bit serial format, thus giving them the power to easily wire up the wide datapaths required to build a contemporary microprocessor. The kit also features an embedded controller which manages kit functions and provides support for a boundary-scan style netlist check of the student's wiring for easy debugging. FPGAs in the device array are easily upgraded, and a programmable clock generator is provided so clock speeds can scale up to 100 MHz as FPGA technology progresses.

# XPUTER / Prototype MoM-3

**FPGA Devices:**
2 XC4000E(X)
1x XC4010
8x rDPA-1

**On-board RAM:**
2MB of SRAM implemented, up to 4GB extendable

**External bus:**
VME-Bus

**Interconnect:**
smart memory interface (SmIF) & internal bus, called MoM-bus

**Contact:**
Reiner W. Hartenstein
University of Kaiserslautern
Department of Computer Science
Erwin-Schroedinger-Strasse
D-67663 Kaiserslautern, Germany
Phone: ++49 631 205 2606
Fax: ++49 631 205 2640
mailto:abakus@nospam.informatik.uni-kl.de
URL: http://xputers.informatik.uni-kl.de

**Notes:**
Xputers are procedurally data-driven custom computing machines (PDD-CCMs), based on a non von Neumann execution mechanism. A wide variety of computation-intensive applications can be acclerated. Xputers are universal and are usable stand-alone or as accelerators.
The Xputer paradigm supports a wide variety of data paths without needing to change the sequencer(s) - in contrast to von Neumann.
For info on principles see:
http://xputers.informatik.uni-kl.de/xputer/index_xputer.html for papers about Xputers see:
http://xputers.informatik.uni-kl.de/papers/main.html

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# MORRPH-ISA

**FPGA Devices:**
6 Xilinx Chips (any combination of 4008,4010,4013,4025)

**Additional Logic:**
Each FPGA dedicates 80 pins for connection with user-defined chips. These chips may be memory, arithmetic, interconnect, or other TTL or CMOS chips.

**Interconnect:**
The six FPGAs are configured in a 2x3 mesh network. Up to 24-bits are used for each North, South, East, and West interconnection bus.

**External Connections:**
At the North, East, and West edges of the array, the 24-bit busses connect to ribbon cables through bi-directional buffers. The busses at the South edge of the array interface with the ISA bus though I/O port locations.

**Contact:**
Thomas H. Drayer
Spatial Data Analysis Lab
340 Whittemore Hall
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061 - USA
Phone (703) 231-8657
Fax (703) 231-3362
Email: tdrayer@nospam.birch.ee.vt.edu

**Notes:**
13 prototype printed circuit boards are currently being manufactured. As demand requires, additional units will be fabricated for university or industrial research. See FCCM '95 proceedings for more detailed desc of the architecture. A sophisticated development system (with partitioning and global routing) for image processing design creation is nearing completion.
Recent articles about the MORPH board may be downloaded from

ftp://mustang.ee.vt.edu in the "PUB" directory.

## MALLEABLE SIGNAL PROCESSOR version 0 (MSP-0)

**FPGA Devices:**

2 socketed Altera EPF10K100GC503DX-3 CPLDs.

**On-board RAM:**

6144K 20 nS SRAM organized as one bank of 512Kx48 bits or two banks of 512Kx24 bits per CPLD.

**External busses:**

Per CPLD:
Three 40-bit Quad C40 DSP VME board busses.
One 80-bit Front or 80-bit Back bsu (depending on CLPD board position).
Four dedicated inputs (spare FPGA pins).

**Interconnect:**

80-bit Inter-PLD bus, user defineable for n-bit pipelines, global busses, rings, virtual inputs. Throughput is dependent on implementation.

**Clocks:**

2 low skew clocks are provided per CPLD, with one spare external. These can be used as with the internal PLL in each device to run the CPLD clock-lock or clock-boost function.

**Contact:**

Jon Alexander Great River Technology
3655 Carlisle Blvd NE
Albuquerque, NM 87110
Phone: 505 881 6262
FAX: 505 837 1620
EMail : jalexand@nospam.greatrivertech.com
URL : http://www.greatrivertech.com

**Notes:**

The Malleable Signal Processor version 0 (MSP-0) is an industry standard VME 9U board with two socketed 10K100 CPLDs. There is also a configuration personality manager which contains a PIC microcontroller, an Altera EPM7128S CPLD, !6 Meg of Intel Flash (for up to 8 program personalities), and Altera EPC1 serial PROMS (for two personalities). All of the MSP-0 board I/O goes through fast 74FCT245E devices. A PMC slot is also available. The 10K100 can be used as hardware accelerators, pre-processors, embedded processors, or hardware algorithm benchmarking.

## Mushroom

**FPGA Devices:**

7 Xilinx 3090

**On-board RAM:**

5Mb 35ns static RAM

**External bus:**

VME (Sun 3/110 as host)

**Interconnect:**

Fixed busses

**Contact:**

Mario Wolczko
now at : Sun Microsystems Labs
Mario.Wolczko@nospam.sun.com
or
Ifor Williams
now at: ADC, 100140.2651@nospam.CompuServe.COM
Project was based at the University of Manchester,
England, 1987-92.

**Notes:**

See: `Using FPGAs to Prototype New Computer Architectures,' Ifor Williams, in `FPGAs', Abingdon EE&CS Books, edited by Will R Moore and Wayne Luk, 1991, pp 373-382. Mushroom was a prototypical implementation of a RISC architecture designed to support dynamic object-oriented languages.

## nfXboard

**FPGA Devices:**
1 Intel NFX780 in 84-pin PLCC
**On-board RAM:**
None
**External bus:**
IBM-PC printer port
**Interconnect:**
None
**Contact:**
XESS Corp.
1-800-549-XESS
devb@nospam.vnet.net
**Notes:**
The nfXboard is a small 4"x 2" board containing an Intel NFX780 FPGA in 84-pin PLCC package. The nfXboard is programmed using the PLDasm HDL and Intel's free PLDshell Plus programming environment. Configuration files are downloaded to the nfXboard through the PC printer port using the JTAG protocol. Additional signals from the printer port can be used to exercise the downloaded design and the results can be observed using the 7-segment LED on the nfXboard. The nfXboard can be used stand-alone or it can be mounted in a protoboard (all 84 pins are made available on two rows of 42 pins each). Since configuration is done using a JTAG stream, it is easy to cascade multiple nfXboards to experiment with larger designs. Inter-FPGA wiring has to be added manually, however. A book accompanies the nfXboard:
"FPGA Workout: Beginning Exercises with the Intel FLEXlogic FPGA". Softcover, 240 pp., 120 illustrations, and index. ISBN 0-9642187-0-4.
This book shows how to use FPGAs to build digital systems ranging from simple combinational logic up to a 4-bit microcontroller. All PLDasm examples in the book can be downloaded into the nfXboard and tested.
The nfxboard has been replaced by newer hardware. See the XESS web site for further information.

## nP

**FPGA Devices:**
2 Xilinx 3090
**On-board RAM:**
64K SRAM / 1M DRAM
**External bus:**
ISA
**Interconnect:**
Fixed
**Contact:**
National Technology, Inc.
9500 South 500 West Suite #104
Sandy, UT 84070
Phone: (801) 561-0114
FAX: (801) 561-4702
Email: bruceg@nospam.metalith.com
**Notes:**
The nP the Nano Processor (nP) is an early commercially available board from NTI.

## PCI Pamette V1

**FPGA Devices:**
4 XC4010E
**On-board RAM:**
Two 64k x 16-bitsSRAM banks

4 angled 72-pin SIMM DRAM connectors

**External bus:**
PCI

**Interconnect:**
2x2 matrix of PQ208 footprints

**Contact:**
Mark Shand
shand@nospam.pa.dec.com

**Notes:**
See: http://www.research.digital.com/SRC/pamette

---

## perle-0

**FPGA Devices:**
25 Xilinx 3020

**On-board RAM:**
0.5 MB

**External bus:**
VME

**Interconnect:**
Fixed mesh

**Contact:**
Patrice Bertin
Paris Research Laboratory
Digital Equipment Corporation
85, avenue Victor Hugo
92500 Rueil-Malmaison, France
bertin@nospam.prl.dec.com or
Partice.Bertin@nospam.inria.fr

**Notes:**
The first board from the Programmable Active Memories (PAM) project at DEC PRL. Replaced by the DEC PAM perle-1.

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## perle-1

**FPGA Devices:**
24 Xilinx 3090

**On-board RAM:**
4MB SRAM

**External bus:**
DEC TURBOchannel

**Interconnect:**
Fixed mesh

**Contact:**
Patrice Bertin
Paris Research Laboratory
Digital Equipment Corporation
85, avenue Victor Hugo
92500 Rueil-Malmaison, France
bertin@nospam.prl.dec.com or
Partice.Bertin@nospam.inria.fr

**Notes:**
The second board from the Programmable Active Memories (PAM) project at DEC PRL. Set the record for RSA encryption in 1990. More information is available at http://pam.inria.fr/.

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## PRISM

**FPGA Devices:**
4 Xilinx 3090

**On-board RAM:**
None
**External bus:**
16 bit
**Interconnect:**
None
**Contact:**
Mike Wazlowski or Harvey Silverman
Laboratory for Engineering Man/Machine Systems
Brown University
Providence, RI 02912
{mew,hfs}@nospam.lems.brown.edu
**Notes:**
The Processor Reconfiguration through Instruction Set Metamorphosis (PRISM) is notable for its use of C as the description language for the programmable logic.

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## PRISM-II

**FPGA Devices:**
3 Xilinx 4010 per processing node
**On-board RAM:**
128K x 32 per 4010
**External bus:**
64 bit writes, 32 bit reads, on processor bus (it's not external)
**Interconnect:**
Inverted tree, or none, application selectable
**Contact:**
Mike Wazlowski or Harvey Silverman
Laboratory for Engineering Man/Machine Systems
Brown University
Providence, RI 02912
{mew,hfs}@nospam.lems.brown.edu
**Notes:**
Each Processor Reconfiguration through Instruction Set Metamorphosis (PRISM-II) board is a node in the Armstrong III loosely-coupled parallel processor. The host CPU is a 33Mhz AMD Am29050 RISC processor. There are 20 nodes that are connected by a reconfigurable (of course) interconnection topology.

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## ProBoard

**FPGA Devices:**
12 PROTEUS (Custom designed SRAM-base FPGA)
**On-board RAM:**
4 dual-port RAMs (8K x 16bit x 4)
**External bus:**
Original bus
**Interconnect:**
2 opposing groups of PROTEUS chips (6 PROTEUS for each direction)
**Contact:**
Kazuhiro Hayashi
NTT Optical Network Systems Laboratories
1-2356 Take Yokosuka-shi
Kanagawa 238-03 JAPAN
Email: kazu@nospam.exa.onlab.ntt.jp
**Notes:**
Line interface modules for ProBoard: 156Mbps X 4 Optical interface, 6.3Mbps X 2 coaxial cable interface with clock recovery circuit using time stamp method, 1.5Mbps X 2 metalic cable interface with clock recovery circuit using time stamp method, and HIPPI interface.

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# P Series Virtual Computer

**FPGA Devices:**
52 - Xilinx XC-4010E-4 FPGA OR Xilinx XC-4013E-3 FPGA -- P4 Series
40 - Xilinx XC-4010E-4 FPGA OR Xilinx XC-4013E-3 FPGA -- P3 Series
26 - Xilinx XC-4010E-4 FPGA OR Xilinx XC-4013E-3 FPGA -- P2 Series
14 - Xilinx XC-4010E-4 FPGA OR Xilinx XC-4013E-3 FPGA -- P1 Series
**On-board RAM:**
8 MB SRAM 256K dual-ported SRAM -- P4 Series
6 MB SRAM 256K dual-ported SRAM -- P3 Series
4 MB SRAM 256K dual-ported SRAM -- P2 Series
2 MB SRAM 256K dual-ported SRAM -- P1 Series
**Interconnect:**
24 - ICUBE Programmable Interconnect Devices -- P4 Series
18 - ICUBE Programmable Interconnect Devices -- P3 Series
14 - ICUBE Programmable Interconnect Devices -- P2 Series
12 - ICUBE Programmable Interconnect Devices -- P1 Series
**External bus:**
Bus Independant
Currently --- Single Slot SBus Plugin Interface Board for SUN Workstation Compatible Computers
**Contact:**
John Schewel
Virtual Computer Corporation
6925 Canby Ave #103
Reseda CA 91335 USA
Email: jas@nospam.vcc.com
Tel: (818) 342-8294 Fax: (818) 342-0240
Visit Our Web Site at: VCC's Home Page

**Notes:**
The **P Series Virtual Computer$^{tm}$ (P4)**, is a single board desktop reconfigurable computer. The P Series, with massive reconfigurable logic (over 650,000 logic gates), delivers supercomputer performance and speed at a fraction of the cost of a supercomputer. The P-Series Virtual Computer plugs into existing computer systems via an interface card. (SBus Compatable Workstation currently available.)
More information on the P Series Virtual Computer is available at: VCC's Website for the P Series Virtual Computer.

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# R16

and

# RISC4005

**FPGA Devices:**
1 Xilinx XC4005 or larger XC4000 series device
**On-board RAM:**
64K Words (16 bit words)
**External bus:**
R16 bus, 16 bit addr, 16 bit data, Synchronous at 20 MHz
**Interconnect:**
Any
**Contact:**
Philip Freidin
Fliptronics
468 S. Frances St,
Sunnyvale, CA 94086
Phone: (408) 737-8060
email: fliptron@nospam.netcom.com
**Notes:**
A 16 bit RISC processor that requires 75% of an XC4005, 16 general registers, 4 stage pipeline, Target speed is 20 MHz. Can be integrated with peripherals on 1

FPGA, and ISET can be extended. Instruction set is similar to AMD 29000 RISC, and includes 3 address instructions like ADD R4,R7,R12 as well as two and one address instructions. Memory interface is a pipelined load/store operation. I/O space can be upto 64K of 16bit I/O locations. Software currently includes a macro assembler, gate level simulator, ANSI C compiler (but no linker yet), and a debug monitor.

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## Rasa

**FPGA Devices:**
3 Xilinx 4010
**On-board RAM:**
320K SRAM
**External bus:**
ISA
**Interconnect:**
2 Aptix FPICs
**Contact:**
Herman Schmit
ECE Department
Carnegie Mellon University
Pittsburgh, PA 15213
Phone: (412) 268-2476
**Notes:**
Integrated with a behavioral synthesis tool which allows specification of the desired algorithm in behavioral Verilog or C.

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## RC1000-II

**FPGA Devices:**
Xilinx XC4010E
**On-board RAM:**
256KB, 1MB SRAM. Industry Pack Modules.
**External bus:**
ISA
**Input / Output:**
Single slot Industry Pack carrier.
**Contact:**
Embedded Solutions Ltd.
83 Gipsy Lane
Wokingham
Berks
RG40 2BW, UK
E-mail sales@nospam.embedded-solutions.ltd.uk
**Notes:**
The RC1000-II is a supported target platform for the Handel-C V2.0 programming language. Unlike other programming languages, the output of this compiler is not a binary file; it is a net list. The Handel-C tools enable a software engineer to target directly FPGAs in a similar fashion to classical microprocessor cross-compiler development tools, without recourse to a Hardware Description Language. Thereby allowing the software engineer to realise directly the raw real-time processing capability of the FPGA. With Handel-C complete systems can be designed as a programming task, using only conventional and easily available programming skills. Source code and schematics are commercially available for the RC1000-II to enable OEMs to rapidly produce custom variations of the design. More information is available at: http://www.embedded-solutions.ltd.uk

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## RC1000-PP

**FPGA Devices:**
Xilinx XC4085XL or XC40125XV and future package compatible devices.

**On-board RAM:**
8MB of SRAM
**External bus:**
PCI
**Interconnect:**
2 x PMC daughter-board sites and a 50 pin unassigned header
**Contact:**
Embedded Solutions Ltd. 83 Gipsy Lane
Wokingham
Berks
RG40 2BW, UK
E-mail: sales@nospam.embedded-solutions.ltd.uk
**Notes:**
The RC1000-PP hardware platform is a standard PCI bus card. The 8Mb of SRAM are directly connected to the FPGA in four 32 bit wide memory banks. The memory is also visible to the host CPU across the PCI bus as if it were normal memory. Each of the 4 banks may be granted to either the host CPU or the FPGA at any one time. Data can therefore be shared between the FPGA and host CPU by placing it in the SRAM on the board. It is then accessible to the FPGA directly and to the host CPU either by DMA transfers across the PCI bus or simply as a virtual address.

The board is equipped with two industry standard PMC connectors for directly connecting other processors and I/O devices to the FPGA; a PCI-PCI bridge chip also connects these interfaces to the host PCI bus, thereby protecting the available bandwidth from the PMC to the FPGA from host PCI bus traffic. The 50 pin unassigned header is provided for either inter-board communication, allowing multiple RC1000-PPs to be connected in parallel or for connecting custom interfaces.

The support software provides Windows®95 and NT®4.0+ drivers for the board, together with application examples written in Handel-C, or the board may be programmed using the Xilinx XACTstep™ tools and other EDA tools. More information is available at: http://www.embedded-solutions.ltd.uk

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## Reconfigurable Neural Network Server

**FPGA Devices:**
16 x (one 3064, four 3042, two 3020/3030, all Xilinx)
**On-board RAM:**
None accessible from the FPGAs
16 MByte DRAM, 2 MByte SRAM on each processor bus
4 32-bit wide FIFO-channels between processor and FPGAs
**External bus:**
VME, special designed communication streams controlled by FPGAs
**Interconnect:**
Some fixed buses
**Contact:**
Jon G. Solheim
Department of Computer Systems and Telematics
Norwegian Institute of Technology
N-7034 Trondheim
email: jon@nospam.idt.unit.no
**Notes:**
RENSS is a special purpose computer for Neural Networks. It has 16 TMS320C30-33 as processing elements, and a dynamic reconfigurable communication system. The FPGAs are accessible from the processor, and thereby usable for implementing co-processor routines in hardware, as well as intelligent communication (mixing communication and computation). All FPGAs are configured the processor.

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## RHO

**FPGA Device:**
1 Xilinx XC6216

**On-board RAM:**
None
**External bus:**
PS2 (bidirectionnal) parallel port
**Interconnect:**
multi I/O (with a miniature 50 pins connector)
**Contact:**
Jean Conter
ENSEEIHT Informatique-équipe VPCAB
2 rue Camichel
31071-TOULOUSE-FRANCE
Email: conter@nospam.enseeiht.fr

**Notes:**
RHO: Reconfigurable Hardware Overdrive
It is probably the smallest implementation of the XC6216 RPU : one GAL (16V8), one oscillator (DS1075), two latches and a XC6216HT144 have been placed on a dongle sized board (45*45 mm).
This 'coprocessing dongle' connects directly to a regular parallel port. An interactive development system based on the MDL language is under completion.
The direct I/O access provides a simple solution for developping logic analyzers, pulse pattern generators and general purpose interfaces (image processing, cryptography,...)

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## RIPP

(See RIPP10 update below)

**FPGA Devices:**
8 Altera FLEX 81188
**On-board RAM:**
2 MB SRAM
**External bus:**
ISA
**Interconnect:**
Fixed buses / programmable interconnect (see Description)
**Contact:**
Nick Tredennick
Altera Corporation
2610 Orchard Parkway
San Jose, CA 95134-2020
Phone: (408) 894-7000
Email: nickt@nospam.altera.com
**Notes:**
The Reconfigurable Interconnect Peripheral Processor (RIPP) contains up to 8 Altera FLEX 81188 parts, each of which may be replaced by an ICUBE IQ160 Field Programmable Interconnect Device (FPID). Devices are grouped into 4 pairs of 2 devices, each sharing an SRAM device. Designed by David E. Van den Bout of the Anyboard project.

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## RIPP10

**FPGA Devices:**
8 Altera FLEX EPF81188
**On-board RAM:**
2 MB SRAM
**External bus:**
ISA
**Interconnect:**
Fixed buses
**Contact:**
Stephen Smith

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Tel: (408) 544-7666
E-mail: sjsmith@nospam.altera.com
WWW Page: http://www.altera.com/html/programs/phd.html

**Notes:**

The Reconfigurable Interconnect Peripheral Processor (RIPP10) contains up to 8 Altera FLEX 81188 parts and four SRAM devices. Devices are grouped into 4 pairs of 2 devices, each sharing an SRAM device. Designed by David E. Van den Bout of the Anyboard project. These platforms are available for free to qualified researchers.

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## RPM

**FPGA Devices:**

7 Xilinx XC4013/board, total of 9 boards

**On-board RAM:**

2 MB SRAM controlled by 2 XC4013s (first level memory/cache)
8 MB SRAM controlled by 3 XC4013s (second level memory/cache)
96 MB DRAM controlled by 2 XC4013s (third level memory)

**External bus:**

SCSI connection to a Sun SPARC host, custom on-board bus and backplane FutureBus+.

**Interconnect:**

??

**Contact:**

Michel Dubois
Dept. of Electrical Engineering - Systems
University of Southern California
Los Angeles, CA 90089-2562
Email: dubois@nospam.paris.usc.edu

**Notes:**

The USC Rapid Prototyping engine for Multiprocessors (RPM) is used for multiprocessor experimentation. A preprint of a report to appear on IEEE Computer Magazine in February 1995 obtained through ftp.
A homepage for the USC RPM is also available.

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## S56X2

**FPGA Devices:**

1 Xilinx 3064 or optional 3042

**On-board RAM:**

128KW(24-bit) (shared with DSP56002)

**External bus:**

SBus & Flexible

**Interconnect:**

See notes below.

**Contact:**

Michael C. Peck
President
Berkeley Camera Engineering
1122 B Street, Suite 219
Hayward, CA 94541-4227
Phone: 510-889-6960
Fax: 510-889-7606
email: mikep@nospam.bce.com

**Notes:**

The S56X2 is an SBus card that contains a 66MHz Motorola 56002 DSP, a Xilinx 3064 memory 128K words (24-bits) SRAM. The 3064 sits directly on the 56002 memory bus and has a DC37F connector to the outside world for user defined I/O. New to the S56X2 version is RS-422 I/O (4 pair out, 4 pair in) between some of the Xilinx and the DC37F pack panel connector. The Xilinx can be accessed from the

56002 with two signals mapped from the SBus through the PAL.

Replaces DSP-56X.

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## SBX+

**FPGA Devices:**
Choice between any Xilinx 208 pin part or Altera 240 pin part. Up to four in any combination.
**On-board RAM:**
0.5 MB of SRAM
**External Bus:**
PCI or SBus
**Interconnect:**
Local bus and up to 87 additional lines.
**Contact:**
stuart.adams@nospam.east.sun.com
**Notes:**
Current Xilinx boards have been populated with XC4013E. Bare boards are available for other devices. More information available at: SBX+

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## SLC1655

**FPGA Devices:**
Portable VHDL design allows operation on Lucent, Altera or Xilinx. Requires less than 20% of gates on larger FPGA devices. Evaluation board uses 80% of gates on a Lucent OR2CA15 device (including RAM and ROM).
**On-board RAM:**
512 x 12 instruction ROM, 32 bytes RAM. RAM and ROM can be scaled up or down to fit budget and application.
**External bus:**
Microcontroller type parallel ports.
**Interconnect:**
Typical Microcontroller I/O via three 8-bit I/O ports. Device is intended to form a custom microcontroller on a single FPGA.
**Contact:**
Wade Peterson, Silicore Corporation
3525 East 27th Street, No. 301
Minneapolis, MN 55406
e-mail: peter299@maroon.tc.umn.edu
web page: http://www.silicore.net/
**Notes:**
8-bit RISC processor delivered as synthesizable VHDL soft core. This device is 100% software compatible with the PIC16C55 ('PIC(tm)' processor) from Microchip Technology. Design can be scaled up or down to match other processors in the same family. Assembler, 'C', Fuzzy Logic and BASIC software tools available. Microcomputer instructions reside in ROM inside of FPGA. A VHDL parallel port interface is included to support application code development through a PC-compatible parallel port interface (software included). Evaluation board available.

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## SPARXIL

**FPGA Devices:**
3 Xilinx XC4010s
**On-board RAM:**
2 256Kx32bit SRAMs for user data 1 128Kx8bit SRAM for on-board configuration cache
**External bus:**
SBus
**Interconnect:**

Fixed

**Contact:**

Andreas Koch
Institut f"ur theoretische Informatik
Abteilung Entwurf Integrierter Schaltungen
Gaussstr. 11
D-38106 Braunschweig, Germany
Email: a.koch@nospam.tu-bs.de

**Notes:**

See FPL'93 Oxford workshop

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## SPACE

**FPGA Devices:**

16 Algotronix CAL1024

**On-board RAM:**

4 MB DRAM (not directly connected to CAL1024s)

**External bus:**

Custom / 10 Mbps Transputer serial links

**Interconnect:**

Fixed grid with expansion to other boards

**Contact:**

George Milne
Advanced Computing Research Centre
University of South Australia
The Levels, SA 5095
Australia
E-mail: *milne@nospam.cis.unisa.edu.au*
Telephone: +61 8 8302 3943

**Notes:**

The Scalable Parallel Architecture for Concurrency Experiments (SPACE) is used for research into reconfigurable computers taking advantage of run-time reconfiguration. Simulation of physical systems modelled as cellular automata, and high speed, adaptive information filtering are two such applications. Design entry is through a Macintosh layout editor, Caledonia. A hardware operating system and shell are used for scriptable configuration and system testing. See our Reconfigurable Computing page. *SPACE is no longer being built, and has been replaced by SPACE 2* .

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## SPACE 2

**FPGA Devices:**

8 Xilinx XC6216/XC6264

**On-board RAM:**

32 MB, 12 ns SRAM SIMMs

**External bus:**

64-bit @ 33 MHz PCI (host-board) / 2 x 64-bit @ 50 MHz overhead backplane

**Interconnect:**

2-D toroidal mesh on each board; fixed network to multiple boards

**Contact:**

Bernard Gunther
Advanced Computing Research Centre
University of South Australia
The Levels, SA 5095
Australia
E-mail: *gunther@nospam.cis.unisa.edu.au*
Telephone: +61 8 8302 3986

**Notes:**

This is the second generation Scalable Parallel Architecture for Concurrency Experiments (SPACE). SPACE 2 is a modular reconfigurable computing platform designed to accelerate stream-oriented applications, in particular. A complete platform comprises (typically) a DEC Alpha motherboard with multiple 64-bit PCI slots, hosting at least two processing boards. A passive overhead backplane, carrying

two 64-bit board-to-board links, a 17-bit global bus and global clocks, connects the processing boards to form large systems with effectively multiple access ports to the processing board RAM. Each processing board holds 8 XC6216 FPGAs (and soon, XC6264 devices) for computing, and a XC4025E for PCI interface and central control. The toroidal mesh connecting the computing devices provides four 32-bit east-west paths and two 41-bit north-south paths. With the XC6216 devices a pair of boards contains a total of 64-k cells, or approximately a quarter of a million NAND gates equivalent; this capacity will approach 1 million gates equivalent with the pin-compatible XC6264 devices installed.

From 4 MB to 32 MB of 12 ns SRAM SIMMs is available for use as a fast buffer (minimum 200 MB/s bandwidth), general-purpose storage, or to hold configuration contexts. The host processor can access the RAM at 64-bit width, while the FPGAs are limited to 32-bit accesses. Vector address counters in the control logic enable users to transfer vectors to the FPGAs under programmable control, with the option of interrupting the host upon completion. Programmable clock, pulse train, and pulse generators drive the XC6200 global clocks at up to 66 MHz. To speed up device configuration, a number of complete FPGA edit lists, or configuration data, may be preloaded into the board RAM for later hardware-assisted reconfiguration. The entire context of a single XC6216 FPGA can be saved and swapped with a stored context in under one millisecond.

Under Digital UNIX the SPACE 2 boards appear as regular character device files that can be opened, read/written, and seeked. The on-board RAM and the FPGA configuration spaces are accessible in this way. Hardware designs for the XC6216s may be created in VHDL (Synopsys), schematic (Viewlogic), or at gate level using the Xilinx XACTstep 6000 tools. Alternatively, the Trianus integrated FPGA design system from ETHZ may be used to describe XC6200 circuits in the Lola HDL. SPACE 2 systems (including host, software, and processing boards) are available commercially.

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## Spectrum

**FPGA Devices:**
2 XC4010s on Reconfigurable Interface Card (G800-RIC)
32 XC4013s grouped in XMODules ( -- see Notes below)

**On-board RAM:**
Maximum 128 MB DRAM and 4 MB SRAM ( --See Notes below)

**External bus:**
VESA (VL) Local bus (PCI in September, VME in December)
30 MB/sec memory mapped, 133 MB/sec bus master burst mode
VESA Media Channel)-25 MHz, 32-bit (100 MB/sec) video bus
50 pad VMC edge fingers connect to variety of peripherals
50-pin external connector supports 32-bit I/O devices

**Interconnect:**
130-pin Virtual Bus Architecture programmable for 32-bit pipelines, global busses, isolated busses, rings, meshes
All interconnect via Xilinx 4010's on G800 RIC.
Dataflow specific bandwidths vary from 64-bit global bus @ 17 MHz to 32-bit pipeline @ 76 Mhz. 5 low skew, high quality clocks are provided per FPGA.

**Contact:**
bovarga@nospam.gigaops.com
2374 Eunice St.
Berkeley, CA. 94708
Phone (510) 528-8438
Fax (510) 526-6688

**Notes:**
XMODs have 2 XC4000 series FPGAs on a 2.4" x 3.65" card with 2 100-pin stacking connectors on the top and bottom.
Up to 8 XMODs may be in 1 stack. Up to 16 XMODs or I/OMODs of all types on Giga Ops' G-800 RIC in 4 stacks of 4 each.

X210MOD = 2 x XC4010s, 8 MB DRAM, 256 K SRAM

X213MOD = 2 x XC4013s, 8 MB DRAM, 256 K SRAM
VIDMOD = I/O for Composite, S-Video, PAL, SECAM, R,G,B

16 x X213MODs = 32 XC4013s, 128 MB DRAM, 4 MB SRAM
16 x X210MODs = 32 XC4013s, 128 MB DRAM, 4 MB SRAM
XLINK-OS automates the interface between routed Xilinx configurations and FPGAs. Features include condensing bit files to single executables, loading files to correct correct FPGAs in system, assigning addresses to variables and handling parameter passing.

The Spectrum architecture is open and supported by third party developers. Contact docmgr@nospam.gigaops.com for Spectrum specifications. XMODs may be connected to custom boards or embedded in peripheral devices.

The XC Compiler is a C syntax HDL for Xilinx FPGAs.
The IC Compiler is an ANSI C Compiler for Xilinx FPGAs.
Both compilers are available to qualified researchers.
Video computing, DSP, and I/O libraries are available.

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## Spectrum2

**FPGA Devices on PCI hostbus board (August, 1996):**
2 XC4000E(X) series on Reconfigurable Interface Card (G900RIC). The G900 PCI-RIC implements the Xilinx Logicore™PCI Target and Initiator Modes in Xilinx X4013E or other PQ240 FPGAs. A second PQ240 FPGA is used to execute the robust clocking scheme and for data routing and switching and processing.

**FPGA Devices for Data Processing/Routing/Switching:**
32 XC4000E(X)s series in groups of two on 16 XMODs. Maximum of 640,000 Xilinx gates when XC4020s are used (August, 1996).

**On-board Memories:**
Maximum 128MB DRAM and 4MB SRAM in 16 XMODs. 512KB surface mounted FLASH, 128KB socketed FLASH, 128KB SRAM on G900

**External busses:**
Eight 32-bit busses - maximum 128-bit sustained I/O @33MHz - 80MHz. Four 34-bit I/O ports via 68-pin edge fingers. Four 36-bit I/O ports via 50-pin male IDC connectors.

**Interconnect:**
130-pin Virtual Bus Architecture™ programmable for 32-bit pipelines, global busses, isolated busses, rings, meshes All interconnect is via Xilinx FPGAs on G900 PCI-RIC and is programmable.
Dataflow specific bandwidths vary from 96-bit global busses @ 20 MHz to 32-bit pipelines @ 76 MHz.

**Clocks:**
8 low skew, high quality clocks per XMOD, 5 per FPGA. These can be internal, external, self-clocking data streams, PLLS, FGENs, XTALs, etc.

**Contact:**
bo@nospam.gigaops.com
2510 MLK Way
Berkeley, CA. 94708
Phone (510) 848-5446
Fax (510) 848-5667
WWW: http://www.reconfig.com, click on Sponsors, then on Giga Ops logo.

**Notes:**
XMODs™ hold 2 Xilinx PQ208 FPGAs on a 2.4" x 3.65" card with 2 100-pin stacking connectors on the top and bottom. Up to 8 XMODs may be in 1 stack. Up to 16 XMODs or I/OMODs of all types on Giga Ops' G-900 RIC in 4 stacks of 4 each. XMODs may be embedded in custom computing boards and peripherals.
XC5210MOD = 2 x XC5210s, 8MB DRAM, 256KB SRAM (all MEMs optional)
X210EMOD = 2 x XC4010Es, 8MB DRAM, 256KB SRAM
X213EMOD = 2 x XC4013Es, 8MB DRAM, 256KB SRAM
X220EMOD = 2 x XC4020Es, 8MB DRAM, 256KB SRAM
X228EXMOD = 2 x XC4028EXs, 8MB DRAM, 256KB SRAM

4A/DMOD = 4, 12-bit, 40MHz input channels
4VIDINMOD = 4 NTSC/PAL input channels
4GIGAMOD = 4 1.0625 Fiber Channel Ports VIDMOD = 1 NTSC/PAL I/O channel

**OS Code Generator for Virtual Hardware Architecture™:**

The Spectrum2 Virtual Bus™ enables a wide variety of computing architectures to be implemented. XLINK-OS ™ automates communication interfaces between host apps and Spectrum FPGAs, MEMs, interconnect, and I/O and eliminates the need to write custom drivers for each algorithm or application implemented in a Spectrum Reconfigurable Computing Platform. Features including condensing bit files to single executables, loading files to correct FPGAs in system, assigning addresses to variables, and handling parameter passing.

XLINK-OS and monitor, diagnostic, and I/O Libraries are available as RC-NTDEV-SW (August, 1996) in a WindowsNT environment. The Spectrum architecture is modular, scaleable, reprogrammable, open, and embeddable. Contact docmgr@gigaops.com for the XMOD Design Specification and other papers and presentations.

XL is a language in development at Giga Ops to describe FPGAs.

XL is provided free of charge to Spectrum customers, as is XSCRIPT and the XL Compiler, which generates .XNF files. These tools will be posted as shareware in 1997.

---

## SPLASH

**FPGA Devices:**

32 Xilinx 3090

**On-board RAM:**

4 MB SRAM

**External bus:**

VME

**Interconnect:**

Linear array

**Contact:**

Jeffrey M. Arnold
IDA Supercomputing Research Center
17100 Science Drive
Bowie, MD 20715
Phone: (301) 805-7479
FAX: (301) 805-7602
Phone: jma@nospam.super.org

**Notes:**

Splash has been replaced by Splash 2.

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## SPLASH 2

**FPGA Devices:**

16 Xilinx 4010

**On-board RAM:**

8 MB

**External bus:**

Sun SBus

**Interconnect:**

Linear array plus crossbar

**Contact:**

Jeffrey M. Arnold
IDA Supercomputing Research Center
17100 Science Drive
Bowie, MD 20715
Phone: (301) 805-7479
FAX: (301) 805-7602
Phone: jma@nospam.super.org

**Notes:**

Splash 2 is a successor to Splash.

## Spyder

**FPGA Devices:**
5 Xilinx 4003, 2 Actel A1280
**On-board RAM:**
128K SRAM plus 2K fast registers
**External bus:**
VME and Sun SBus
**Interconnect:**
Fixed
**Contact:**
Christian Iseli
Logic Systems Laboratory
Swiss Federal Institute of Technology
CH-1015 Lausanne
Switzerland
Email: chris@nospam.lslsun.epfl.ch
**Notes:**
A reconfigurable VLIW machine.

## Spyder2

**FPGA Devices:**
3 Xilinx 4008 (upgradable to 4010), 2 Xilinx 4005, 1 Actel A1280 and 1 Actel A1225
**On-board RAM:**
128K SRAM plus 4K fast registers
**External bus:**
VME
**Interconnect:**
Fixed
**Contact:**
Christian Iseli
Logic Systems Laboratory
Swiss Federal Institute of Technology
CH-1015 Lausanne
Switzerland
Email: chris@nospam.lslsun.epfl.ch
**Notes:**
A reconfigurable VLIW machine. A newer version of Spyder.
See: http://lslwww.epfl.ch/Staff/CI for more information.

## The Stack

**FPGA Devices:**
8 iFX 780
**On-board RAM:**
4-8x 8kx24 Fast Sram
**External bus:**
Proprietary 16 bit NRZ bus designed for extensive cabling
**Interconnect:**
420Mb/s 13/24 bit input bus, 30Mb/s OC bus between all nodes, 600Mb/s memory
**Contact:**
Peter Averkamp
Tech. Univ. of Munich
Physics Dept. E20
James-Franck-Str. 1
D-85748 Garching, Germany
Email: petav@nospam.e20.physik.tu-muenchen.de
**Notes:**

Used in conjunction with GHz ECL logic for on-line data reduction algorithms in subnanosecond Synchrotron Experiments

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## ST-FPGA

**FPGA Devices:**
Up to four XILINX 4xxx/5xxx family 208 pin QFP
**On-board RAM:**
None
**External bus:**
ISA
**Interconnect:**
None
**Contact:**
aaps@nospam.erols.com
**Notes:**
The ST_FPGA system is a family of FPGA development modules which can be used stand alone or mounted on a PC ISA BUS carrier board. Each module consists of up to four XILINX 4xxx/5xxx family 208 pin QFP chips. Up to two modules (8 FPGAs) can be mounted to each carrier board to provide a tremendous amount of flexible FPGA power (Up to 160,000 gates). Each ST-FPGA module can be used stand alone, and has power and over 200 IO and monitoring pins. The ST-FPGA SYSTEM comes with download software and sample VHDL and C code and is ideal for ASIC development.
See http://www.erols.com/aaps/ for more information.

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## Tao

**FPGA Devices:**
Xilinx 4000E in base, user's choice in computation array
**On-board RAM:**
4-8 MB SSRAM buffers plus address generators
**External bus:**
PCI
**Interconnect:**
Toroidal Mesh
**Contact:**
bunnie@nospam.mit.edu
**Notes:**
Tao is a high performance platform for implementing reconfigurable hardware designs. The architecture features a high aggregate throughput and a modular processor core consisting of four reconfigurable macrofunction units embedded in a toroidal interconnect matrix. The modular core allows the platform to be upgraded as reconfigurable hardware technology progresses. A high aggregate throughput is achieved by striking a balance of bandwidth among all the datapath elements, from the PCI bus interface to the intelligent buffers called reformatting engines, to the processor core itself. The platform also features an embedded microcontroller for the support of dynamic reconfiguration schemes. Tao was implemented on a double height PCI card using Xilinx XC4013E-3 FPGAs as the base reconfigurable hardware technology.
See http://web.mit.edu/bunnie/www/tao.html for more information.

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## TbC-Pamette

**FPGA Devices:**
1 to 4 Xilinx 40XX in PQ-208 package Currently supported configurations: 4010 + 4003H 4 x 4010
**On-board RAM:**
Daughter board (see notes)
**External bus:**

DEC TURBOchannel

**Interconnect:**

Fixed mesh 2 x 2 matrix

**Contact:**

Mark Shand
Paris Research Laboratory
Digital Equipment Corporation
85, avenue Victor Hugo
92500 Rueil-Malmaison, France
shand@nospam.prl.dec.com or
shand@nospam.acm.org

**Notes:**

128 user I/O to daughter board. Synchronous RAM daughter board is under development. Pamette is targeted as a generic I/O adapter with local compute capability. This hardware is from the Programmable Active Memories (PAM) project at DEC PRL.

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## TERAMAC

**FPGA Devices:**

108 custom FPGA devices/board

**On-board RAM:**

32MB SRAM/board

**External bus:**

SCSI

**Interconnect:**

1 to 16 board system, hardwired design independent 27 chip, 39 layer MCM

**Contact:**

Rick Amerson
Hewlett-Packard
1501 Page Mill Road
Palo Alto, CA 94304
Email: amerson@nospam.hpl.hp.com

**Notes:**

Approx 64K gates/board. Designed for rapid turnaround of designs to allow investigation of alternative computing ideas. A program protects hardware from bad designs which might damage it. Simulation only, no in-circuit emulation. 100% automatic place and route. System compiles in under ten seconds per chip. See FCCM'95 for details.

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## TM-1

**FPGA Devices:**

4 Xilinx 4010

**On-board RAM:**

4 32Kx9 SRAMs

**External bus:**

Custom to SUN workstation

**Interconnect:**

Entirely programmable using Aptix AX1024 FPIC

**Contact:**

Jonathan Rose
Dept. of Electrical and Computer Engineering
University of Toronto
10 King's College Road
Toronto, Ontario
Canada M5S 3G4
Email: jayar@nospam.eecg.toronto.edu

**Notes:**

The Transmogrifier-1 (TM-1) was operational between 1994 and 1996. It was intended more for rapid prototyping of circuits, but could be used for computing. A technical report on the TM-1 is available on-line. The Transmogrifier C compiler was

used to produce circuits for the TM-1, and is freely available.

## Transmogrifier-2

**FPGA Devices:**
2 to 32 Altera 10K50 (10K100 soon)
**On-board RAM:**
4 to 64 banks of ram; each 64 bits wide; each bank is .5 - 2 Mbytes of SRAM or 8-32 Mbytes of DRAM
**External bus:**
Parallel port to SUN workstation plus 64 to 512 pins of general purpose I/O
**Interconnect:**
Completely programmable one-hop routing through modified partial crossbar; takes advantage of circuit locality to decrease backplane complexity; uses Icube IQ320 programmable crossbar chips
**Contact:**
Dave Lewis or Jonathan Rose
Dept. of Electrical and Computer Engineering
University of Toronto
10 King's College Road
Toronto, Ontario
Canada M5S 3G4
Email: {lewis|jayar}@nospam.eecg.toronto.edu
**Notes:**
The Transmogrifier-2 (TM-2) can have between 1 and 16 modules plugged into a backplane. Each module contains 2 FPGAs, 4 banks of RAM, an I/O connector and a slice of the interconnect network. See "The Transmogrifier-2: A 1 Million Gate Rapid Prototyping System" in the FPGA-97 proceedings or visit the TM-2 web site.

A library of stdio-like routines allow a program on the SUN to transparently communicate with a circuit in the TM-2. The Transmogrifier C compiler can be used to produce circuits for the TM-2, and is freely available.

Status as of April 1997: A two module system is working, and a full sized 16 module system (with 10K100s instead of 10K50s) is being constructed. The latter will have a mechanism for high-speed (20ms) re-programming of each board.

## V6502

**FPGA Devices:**
1 Xilinx 4013
**On-board RAM:**
Not applicable
**External bus:**
40 Pin DIP socket to any 6502 motherboard (ex:AppleII-C)
**Interconnect:**
Fixed wire wrapped interconnect
**Contact:**
Eric Ryherd
VAutomation Inc.
71 Spit Brook Rd.
Suite 306
Nashua NH 03060
Email: eric@nospam.VAutomation.com
**Notes:**
From synthesizable VHDL model available from VAutomation. Pin compatible replacement for the Rockwell 6502 8 bit uP

## VA1000

**FPGA Devices:**
2 Xilinx XC4010s
**On-board RAM:**
32K + 256K SRAM
**External bus:**
PC (ISA)
**Interconnect:**
Direct
**Contact:**
Robert Duncan
Eyepoint Engineering
24 Springpoint Road
Castroville, CA 95012
Email: robert.duncan@nospam.xilinx.com
**Notes:**
Real time Ray Casting in a volumetric dataset, rendering shaded perspective images from an arbitrary view within the dataset. Applications include medical imaging, volume rendering, etc.

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## VC

**FPGA Devices:**
Up to 52 Xilinx 4013
**On-board RAM:**
Up to 8 MB SRAM, 256K dual-ported SRAM
**External bus:**
Bus Independent - Current SBus interface
**Interconnect:**
Up to 24 ICUBE FPID
**Contact:**
Steve Casselman
Virtual Computer Corporation
Reseda, CA 91335
Phone: (818) 342-8294
FAX: (818) 342-0240
Email: sc@nospam.vcc.com
**Notes:**
The Virtual Computer P-Series consists of P1, P2, P3 and P4. The P1 has 14 4013s the P2 26 4013s the P3 40 4013s and the P4 has 52 4013s.

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## VIP

**FPGA Devices:**
5 Altera FLEX81500 and 1 Altera MAX7192
**On-board RAM:**
6 64Kx32 SRAM modules with 20 ns access time. Each module is upgradable to a 256Kx32 SRAM module.
**External bus:**
PCI (32 bits, 33.3MHz)
**Interconnect:**
2D torus network with a 2x2 FLEX81500 matrix (processing matrix).
**Contact:**
Jocelyn Cloutier
Département d'informatique et de Recherche opérationnelle
Université de Montréal
C.P. 6128, Succ. Centre-Ville
Montréal, Canada
H3C 3J7
Email: cloutier@nospam.iro.umontreal.ca
**Notes:**
For more informations, look at this WWW site. This project is done in collaboration

with AT&T Bell Labs.

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## VZ80

**FPGA Devices:**
2 Xilinx 4013s
**On-board RAM:**
Not applicable
**External bus:**
40 Pin DIP socket to any Z80 motherboard (ex:TRS-80)
**Interconnect:**
Fixed wire wrapped interconnect
**Contact:**
Gregory Recupero
VAutomation Inc.
71 Spit Brook Rd.
Suite 306
Nashua NH 03060
Email: greg@nospam.VAutomation.com
**Notes:**
From synthesizable VHDL model available from VAutomation. Pin compatible replacement for the Zilog Z80 8 bit uP.

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## Windchime

**FPGA Devices:**
Actel 1020A (1-3 per processor)
**On-board RAM:**
**External bus:**
**Interconnect:**
Mesh connected wormhole routing
**Contact:**
Erik Brunvand
CS Dept.
University of Utah
Salt Lake City, UT, 84112
Email: elb@nospam.cs.utah.edu
Phone: (801)581-4345
FAX: (801)581-5843
**Notes:**
MIMD multiprocessor. Used for self-timed circuit experimentation.

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## X-12

**FPGA Devices:**
12 Xilinx 3195
**On-board RAM:**
384K SRAM (32K per FPGA)
**External bus:**
ISA
**Interconnect:**
Fixed common bus
**Contact:**
National Technology, Inc.
9500 South 500 West Suite #104
Sandy, UT 84070
Phone: (801) 561-0114
FAX: (801) 561-4702
Email: bruceg@nospam.metalith.com
**Notes:**

## XKL-1

**FPGA Devices:**
2 Xilinx XC4010E-3
**On-board RAM:**
2 x 8K x 8 x 36 cache
2 x 8K x 38 pager (TLB)
8K x 36 scratchpad
**External bus:**
XKL proprietary 2Gbit/sec active backplane bus
**Interconnect:**
None
**Contact:**
Product Information
XKL Systems Corp.
8420 154th Avenue NE
Redmond, WA 98052
np-info@nospam.xkl.com
**Notes:**
This is the CPU for the TOAD-1, a 36-bit computer instruction-set compatible with the Digital Equipment Corporation PDP-10 family of computers (best known as the DECsystem-10 and DECSYSTEM-20, defined by the respective operating systems Tops-10 and Tops-20).
The FPGAs are used for all arithmetic, including floating-point and byte-selection operations. (Note: The PDP-10 architecture is word-oriented, with byte size and position within the 36-bit word defined by a pointer word which also contains the word address.)

## XS40 Board

**FPGA Devices:**
1 XILINX XC4000, XC5200, or Spartan FPGA in an 84-pin PLCC
**On-board RAM:**
32 KByte
**External bus:**
IBM-PC printer port, cascade port, 84-pin breadboard bus
**Interconnect:**
FPGA, microcontroller, and RAM share a common data/address bus
**Contact:**
XESS Corp.
1-800-549-XESS
1-919-387-0076
fpga-info@nospam.xess.com
http://www.xess.com/FPGA
**Notes:**
The XS40 Board is a small 5"x 2" board containing a XILINX XC4000, XC5200, or Spartan FPGA in an 84-pin PLCC package, an 8031 microcontroller, and a 32 KByte RAM. The XS40 Board is programmed using XILINX's M1 programming environment. The 8031 is programmed using MetaLink's 8051 cross-assembler or any other assembler or compiler that outputs a standard .HEX object file. FPGA bitstream files are downloaded to the XS40 through the PC printer port using the serial bitstream format. 8031 object code is also loaded into the 32 KByte RAM through the printer port. The FPGA is treated as a reconfigurable peripheral of the 8031. Additional signals from the printer port can be used to exercise the downloaded design. The results can be observed using the 7-segment LED on the XS40 or sent back for display on the PC. The XS40 can be used stand-alone or it can be mounted in a breadboard (all the pins for the FPGA, microcontroller and RAM are made available on two rows of 42 pins each). Since configuration is done using a serial bitstream, it is easy to cascade multiple XS40 Boards to experiment with multiprocessor and multi-FPGA systems.
The XS40 is one of the prototyping boards used in Prentice Hall's new lab book on

digital design, The Practical Xilinx Designer.
This book shows how to use FPGAs to build digital systems ranging from simple combinational logic up to an 8-bit microcontroller. All the examples in the book can be downloaded into the XS40 and tested.
Additional experiments and materials are presented at the XESS web site.

## XS95 Board

**FPGA Devices:**
1 XILINX XC9500 CPLD in an 84-pin PLCC
**On-board RAM:**
32 KByte
**External bus:**
IBM-PC printer port, cascade port, 84-pin breadboard bus
**Interconnect:**
CPLD, microcontroller, and RAM share a common data/address bus
**Contact:**
XESS Corp.
1-800-549-XESS
1-919-387-0076
fpga-info@nospam.xess.com
http://www.xess.com/FPGA
**Notes:**
The XS95 Board is a small 5"x 2" board containing a XILINX XC9500 CPLD in an 84-pin PLCC package, an 8031 microcontroller, and a 32 KByte RAM. The XS95 Board is programmed using XILINX's M1 programming environment. The 8031 is programmed using MetaLink's 8051 cross-assembler or any other assembler or compiler that outputs a standard .HEX object file. CPLD configuration files are downloaded to the XS40 through the PC printer port using the JTAG port. 8031 object code is also loaded into the 32 KByte RAM through the printer port. The CPLD is treated as a reconfigurable peripheral of the 8031. Additional signals from the printer port can be used to exercise the downloaded design. The results can be observed using the 7-segment LED on the XS95 or sent back for display on the PC. The XS95 can be used stand-alone or it can be mounted in a breadboard (all the pins for the CPLD, microcontroller and RAM are made available on two rows of 42 pins each). Since configuration is done using a serial bitstream, it is easy to cascade multiple XS95 Boards to experiment with multiprocessor and multi-CPLD systems.
The XS95 is one of the prototyping boards used in Prentice Hall's new lab book on digital design, The Practical Xilinx Designer.
This book shows how to use CPLDs to build digital systems ranging from simple combinational logic up to an 8-bit microcontroller. All the examples in the book can be downloaded into the XS95 and tested.
Additional experiments and materials are presented at the XESS web site.

## YARDS

**FPGA Devices:**
Xilinx XC4010 and XC3030
**Daughter card:**
Xilinx XC4010 x4, or Altera MAX9000 x2, or PROTEUS (custom) x2
**On-board RAM:**
(Dual-Port SRAM 32Kx8) x4
**External bus:**
VME
**Interconnect:**
I-CUBE IQ320 x2
**Contact:**
Toshiaki Miyazaki
NTT Optical Network Systems Labs
3-1 Morinosato Wakamiya, Atsugi, 243-01, JAPAN
Email: miyazaki@nospam.aecl.ntt.co.jp
Phone: +81 462 40 2158

Fax: +81 462 40 4309

**Notes:**

The YARDS (Yet Another Re-definable System) is a tightly coupled FPGA/MPU system. It comprises three programmable devices, i.e., an RISC-type MPU with memories, programmable interconnect devices, and FPGAs. Using these, this system supports various styles of coupling between the FPGAs and the MPU which are suitable for constructing telecommunications functions. Using the YARDS and the ANT (ATM Network Termination) board, we implemented an Operation, Administration, and Management (OAM) operation on the Asynchronous Transfer Mode (ATM) network, and realized a remote reconfiguration function through the ATM network. See FPGA'97 proceedings for details.

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## Zelig

**FPGA Devices:**

32 XC3090s

**On-board RAM:**

64K x 8 at each node

**External bus:**

Controlled by Transputer

**Interconnect:**

FPGAs arranged in a ring, 8-bit connections to 4 nearest neighbours' memory, 8-bit direct connections to 2 nearest neighbours. Globally controlled by transputer.

**Contact:**

Neil Howard
Dept. Electronics
University of York
Heslington, York YO1 5DD, UK
email: nh@nospam.ohm.york.ac.uk

**Notes:**

Designed and used for cellular automata applications - image morphology, local histogram equalisation, rank filtering. Neural networks also implemented.