Structured Hardware Design

a KARL-based multiplier floorplan design calculus

(DRAFT NOTES)

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*) PowerPoint re-edited later

$$2^i \cdot w = i\ shl(w) \qquad (19.8)$$

means: multiply w by 2^i = shift left w by i bits.

$$i\ shl(w) = -i\ shr(w) \qquad (19.9)$$

means: shift left by i bits = shift right by -1 bits.

$$i\ shl(j\ shl(w)) = (i+j)\ shl(w) \qquad (19.10)$$

means, shift by i, followed by shift by j = shift by i+j.

$$i\ shl(v) + i\ shl(w) = i\ shl(v+w) \qquad (19.11)$$

means, shift by i, then add = add, then shift by i.

from (19.9) and (19.10) we derive:

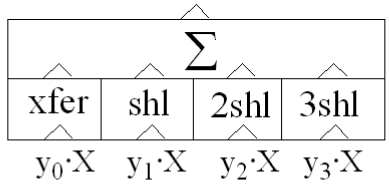
$$i\ shl(w) = j\ shl((j-i)\ shr(w)) \qquad (19.12)$$

$$X = (x_3, x_2, x_1, x_0) \qquad Y = (y_3, y_2, y_1, y_0) \qquad (19.13)$$

produkt P we obtain by:

$$P = \sum_{i=0}^{3} 2^i \cdot y_i \cdot X \qquad (19.14)$$

rule (19.8) converts this to:



(19.15)

$$P = \sum_{i=0}^{3} i \;\; shl(y_i \cdot X)$$

from theorem (19.12) this yields:

$$P = 4\ shl\left(\sum_{i=0}^{3} (4-i\ \ )shr(y_i \cdot X)\right) \qquad (19.16)$$

reverse accumulate sequence i = 0, 1, 2, 3 to 3, 2, 1, 0:

$$P = 4\ shl\left(\sum_{i=3}^{0} (4-i\ \ )shr(y_i \cdot X)\right) \qquad (19.17)$$

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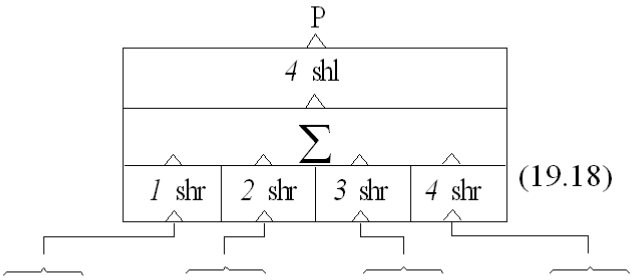

(19.18)

$$P = 4\ \ shl(shr(y_3 \cdot X) + 2\ \ shr(y_2 \cdot X) + 3\ \ shr(y_1 \cdot X) + 4\ \ shr(y_0 \cdot X))$$

The shift left by 4 bits at the exit is not really significant

use rule (19.10) repetitively which yields:

$$P = 4\ \ shl(shr\ (y_3 \cdot X + shr\ (y_2 \cdot X + shr\ (y_1 \cdot X + shr(y_0 \cdot X)))))\qquad (19.19)$$

add C is o.k., as long as C = 0. This yields:

$$P = 4\ \ shl(\underbrace{shr\ (y_3 \cdot X + }_{ConAddShi}\underbrace{shr\ (y_2 \cdot X + }_{ConAddShi}\underbrace{shr\ (y_1 \cdot X + }_{ConAddShi}\underbrace{shr(y_0 \cdot X + C)))))}_{ConAddShi}\qquad (19.20)$$

a regularly structured design, yieldig 4 identical layers *ConAddShi*
Since y_i is a single bit we get the multiplexer insiden *ConAddShi*:

$$y_i \cdot X = \text{if } y_i \text{ then X else 0 endif}\qquad (19.21)$$

The 4 bit integer multiplier demo example fabricated by the MPC (Multi Project Chip) microchip fabrication facilities of the E.I.S. Projekt.