Modeling Dynamically Reconfigurable Systems via Rewriting-Logic (modeling and simulation of the FFT in Optimal Space)

C. Llanos¹,², M. Ayala-Rincón³, R. B. Nogueira³,⁴, R. Jacobi⁵, R. W. Hartenstein⁶

¹Departamentos de Matemática, ²Engenharia Mecânica e ³Ciência da Computação
⁴Universidade de Brasília
⁵Fachbereich Informatik, ⁶Kaiserslautern University of Technology

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Overview (Arvind approach)

- Applying rewriting techniques in hardware design [Arvind et al]
  - specification of correct processors
  - Cache protocols over memory systems
  - Specification of digital circuits
  - Specification and verification of network protocols

Characteristic of Arvind’s approach

- rewriting is neither applied for simulation nor for verification
- Proposal ⇒ Translate to Verilog!

Overview (using Haskell)

- Bejesse et al use Haskell (a functional language) for circuit design, specification and verification
- These ideas are implemented in LAVA system
- This approach shows how the high level abstraction of functional languages is suitable for hardware design

Lava approach takes advantage of high level abstraction provided by functional languages

Overview (Kapur Approach)

- Kapur has used his well-known Rewriting Rule Laboratory - RRL for verifying arithmetic circuits
- RRL is used to verify automatically properties of arithmetic hardware circuits (adders, multipliers, SRT division circuits)

Why Rewriting?

- Rewriting is the formal framework of all functional languages
- This fact allows us to work in more abstract levels
- Rewriting assistant environments help in the task of formal verification of hardware
Rewriting Rules

\[
\text{left side} \rightarrow \text{right side} \quad \text{Premise to be hold}
\]

Rewriting Rule

- Rewriting rules:
  \[ l \rightarrow r \text{ if } C \]
  - Premise to be hold
  - Semantic: "l is replaced by r if C is true"

- Operational semantics:
  a rule is applied to a term, when its left-side matches a sub-term, replacing the matched sub-term with the corresponding right-side of the rule. All that, whenever the premise C of the rule holds.

Specifying Processors

- Basic Processor
  - Single cycle, non pipelined, in-order execution
  - SYS := Sys(MEM,PROC)
  - PROC := Proc(ia, rf, prog)

- AX Architecture
  Instruction set:
  - \( r := \text{Load}(v) \)
  - \( r := \text{Loadpc} \)
  - \( r := \text{Op}(r_1, r_2) \)
  - \( Jz(r_1, r_2) \)
  - \( r := \text{Load}(r_1) \)
  - \( \text{Store}(r_1, r_2) \)

Defining Instruction of the processor by rewriting rules

- Jz-jump-rule:
  \[ Jz(r_1, r_2) \]
  \[ \text{Proc}(ia, rf, prog) \rightarrow \text{Proc}(rf[r_2], rf, prog) \]
  \[ \text{if im}[ia] = Jz(r_1, r_2) \quad \text{and} \quad rf[r_1] = 0 \]

Example: Euclid’s Algorithm for greatest common divisor (GCD)

- GCD Mod Rule:
  \[ \text{Gcd}(a, b) \rightarrow \text{Gcd}(a-b, b) \quad \text{if} \quad (a \geq b) \land (b \neq 0) \]

- GCD Flip Rule:
  \[ \text{Gcd}(a, b) \rightarrow \text{Gcd}(b, a) \quad \text{if} \quad a < b \]

- The term Gcd(6,15) can be reduced by applying the Mod and Flip rules:
  \[ \text{Gcd}(6,15) \rightarrow \text{Flip} \quad \text{Gcd}(15,6) \rightarrow \text{Mod} \quad \text{Gcd}(9,6) \rightarrow \text{Mod} \quad \text{Gcd}(3,6) \rightarrow \text{Mod} \quad \text{Gcd}(3,0) \rightarrow \text{Result}! \]
Characteristic of Rewriting

- Rules are applied non-deterministically
- Controlling the execution of rules can be accomplished by logic

Rewriting-Logic = Rewriting Rules + Strategies

Examples of Rewriting Oriented Environments

- ELAN: it has great flexibility for defining types and ease manipulation of strategies
- Maude: • It’s necessary to do more effort for description
  • it provides model checking useful for hardware verification

Example of a Reconfigurable Architecture

Example of Reconfigurable Architecture

Describing Architectures in ELAN

Problem: how can this architecture be described in ELAN
Using and defining types It’s possible to describe fixed parts and reconfigurable ones

Describing more Complex Architectures

At some time the configuration can be specified

Processor

Example of Reconfigurable Architecture

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How the Execution Process is described in the ELAN system

\[\begin{align*}
\text{[0, port(cPort1), port(cPort2), reg(cReg1), reg(cReg2) # addr1, addr2, const(cConst1), op1, op2]} \\
\text{[0, port(cPort1), port(cPort2), reg(cRegRes1), reg(cRegRes2) # addr1, addr2, const(cConst1), op1, op2]}
\end{align*}\]

where
\[\text{operate(cPort1, cPort2, op1)}\]
\[\text{operate(cReg1, cConst1, op2)}\]

How the Reconfiguration Process is described in ELAN system

\[\begin{align*}
[] \text{reconfigure(MACsArray( [fix0 # rec0] ))}
\end{align*}\]

Using Strategies in ELAN

- Strategies for Proc
- Implicit
- process
- input
- repeat
- (reconfiguration;propagation;execution)
- output
- end

- Using strategies for guiding the application of the rules
- Strategies in ELAN allow to separate execution and reconfiguration steps
- This approach allows a closer specification to transference register description (RTL Description)

Reconfiguration for FFT

\[\begin{align*}
\text{Number of reconfiguration = ln(n) + 1}
\end{align*}\]

An Execution Rule for a pair of MACs

\[\begin{align*}
\text{[MAC01]}
& \Rightarrow [0, port(cPort1), port(cPort2), reg(cReg1), reg(cReg2) # addr1, addr2, const(cConst1), op1, op2]
& \Rightarrow [1, port(cPort3), port(cPort4), reg(cReg3), reg(cReg4) # addr3, addr4, const(cConst2), op3, op4]
\end{align*}\]

where
\[\begin{align*}
\text{operate(cPort1, cPort2, op1)}
\text{operate(cReg1, cConst1, op2)}
\text{operate(cRegRes1, cConst1, op2)}
\end{align*}\]
A Reconfiguration Rule for a pair of MACs

```
[reconfiguration]
<
  [ fix0 ≠ rec0 ]
  [ fix1 ≠ rec1 ]
>
<
  [ fix0 ≠ addr(0),addr(2),const( < 1,0000        0,0000 > ), < + >,< * > ]
  [ fix1 ≠ addr(1),addr(3),const( < 1,0000        0,0000 > ), < + >,< * > ]
```

A Pipelined Reconfigurable FFT
(eliminating the reconfiguration overhead)

While one Mac array is being reconfigured the other array is computing one step of FFT

Advantages of ELAN Environment

- ELAN has the advantage of an embedded inference engine
- A flexible type definition mechanism (data and operators)
- A powerful manipulation of typed expressions through rules and meta-rules
- The availability of logical strategies to control their application.

Conclusions

- The high abstraction of Rewriting Environments makes design exploration easier
- Using ELAN is possible to simulate the description of the architecture
- Descriptions in ELAN are close to the physical architecture