The International Symposium on Low Power Electronics and Design – ISLPED 2006

Rottach-Egern, Germany, Oct 4 - 6, 2006

Chair: Peter Wintermayr

Panel statements by

Reiner Hartenstein

TU Kaiserslautern

Panel Session

Flexibility and Low Power: a Contradiction in Terms? - Can Configurable or Re-Configurable Computing Offer Solutions?

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Wasting Energy by the Internet

did you know ...

... 25% of Amsterdam's electric energy consumption goes into server farms

This is a strategic issue

... a quarter square-kilometer of office floor space within New York City is occupied by server farms

recently the US Senate ordered a study on the energy consumption of servers

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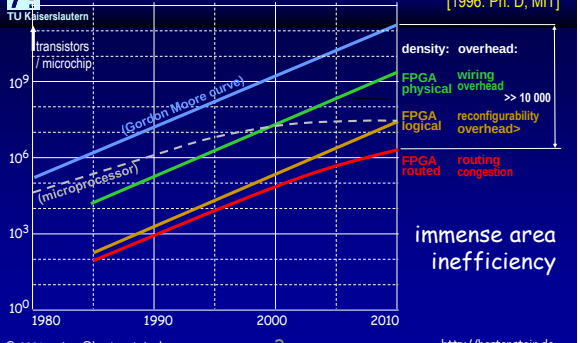
Technology: fine-grained RC: 1st DeHon's Law

[1996: Ph. D, MIT]



immense area inefficiency

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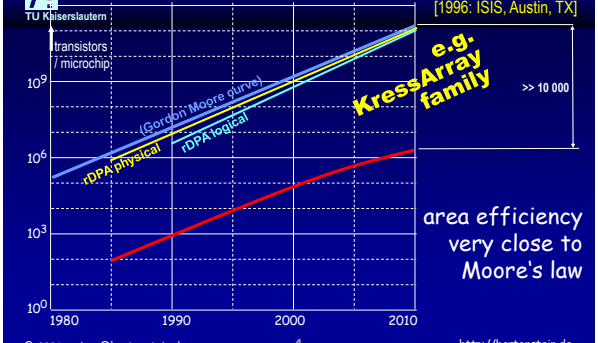
rDPA coarse-grained RC: Hartenstein's Law

[1996: ISIS, Austin, TX]



area efficiency very close to Moore's law

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An Example: FPGAs in Oil and Gas .... (2)

[Herb Riley, R. Associates]

„Application migration [from supercomputer] has resulted in a 17-to-1 increase in performance"

Saves more than $10,000 in electricity bills per year (7¢ / kWh) - .... per 64-processor 19" rack

(Slashing electricity bill to about 10%)

What about higher speed-up factors ?

Coming with more dramatic electricity savings ?

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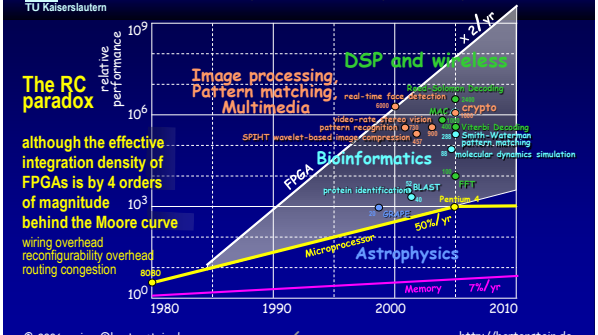
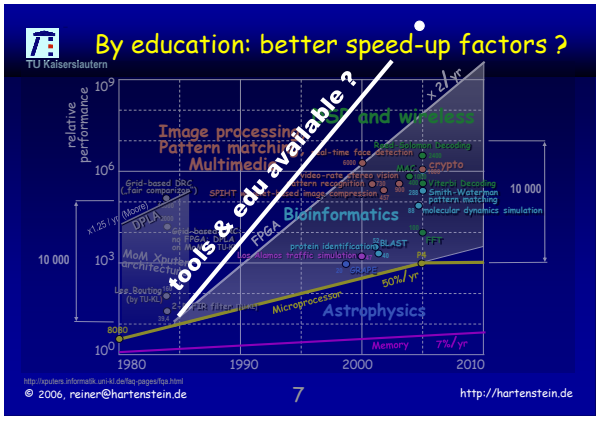
some published speed-up factors

The RC paradox

although the effective integration density of FPGAs is by 4 orders of magnitude behind the Moore curve

wiring overhead
reconfigurability overhead
routing congestion




By education: better speed-up factors ?
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tools & edu available ?
relative performance
Image processing
Pattern matching
Multimedia
DSP and wireless
Bioinformatics
Astrophysics
Memory
7%/ yr
50%/ yr
x 2/ yr
1980
1990
2000
2010
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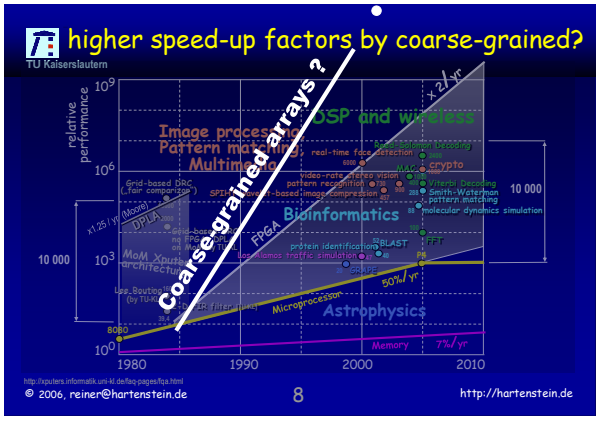
higher speed-up factors by coarse-grained?
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Coarse-grained arrays ?
relative performance
Image processing
Pattern matching
Multimedia
DSP and wireless
Bioinformatics
Astrophysics
Memory
7%/ yr
50%/ yr
x 2/ yr
1980
1990
2000
2010
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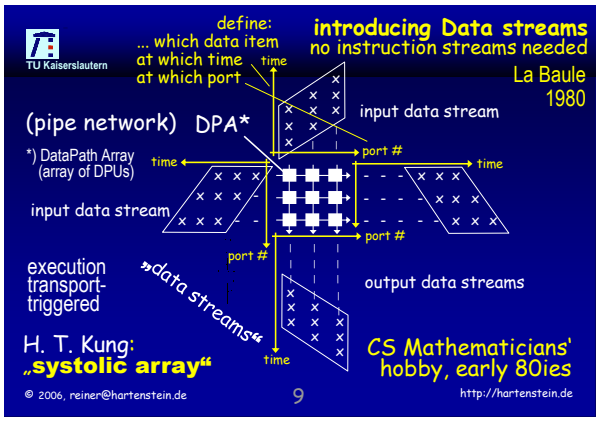
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define:
... which data item
at which time
at which port
introducing Data streams
no instruction streams needed
La Baule
1980
(pipe network) DPA*
*) DataPath Array
(array of DPUs)
input data stream
input data stream
time
port #
execution
transport-
triggered
„data streams"
output data streams
H. T. Kung:
„systolic array"
CS Mathematicians'
hobby, early 80ies
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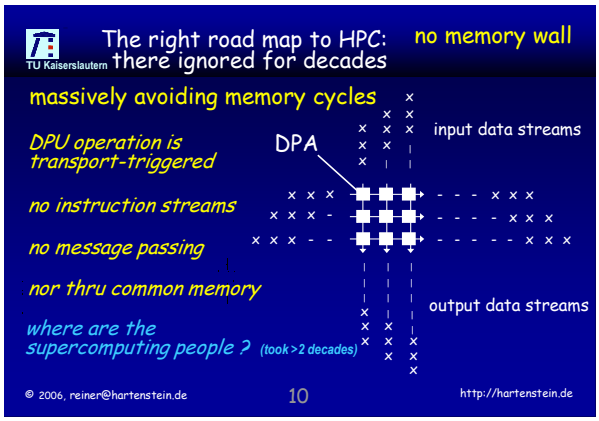
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The right road map to HPC:
there ignored for decades
no memory wall
massively avoiding memory cycles
DPU operation is
transport-triggered
no instruction streams
no message passing
nor thru common memory
where are the
supercomputing people ?
(took >2 decades)
DPA
input data streams
output data streams
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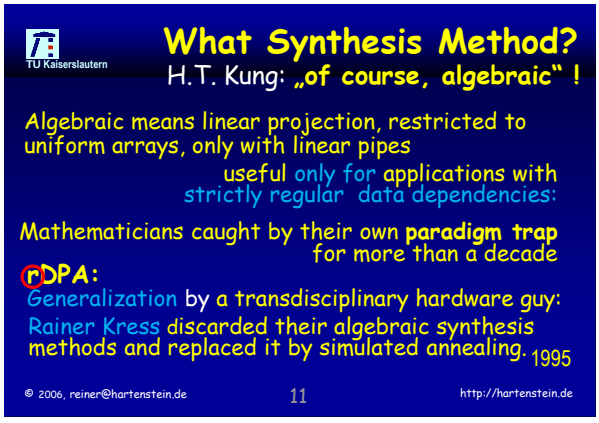
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What Synthesis Method?
H.T. Kung: „of course, algebraic" !
Algebraic means linear projection, restricted to
uniform arrays, only with linear pipes
useful only for applications with
strictly regular data dependencies:
Mathematicians caught by their own paradigm trap
for more than a decade
rDPA:
Generalization by a transdisciplinary hardware guy:
Rainer Kress discarded their algebraic synthesis
methods and replaced it by simulated annealing. 1995
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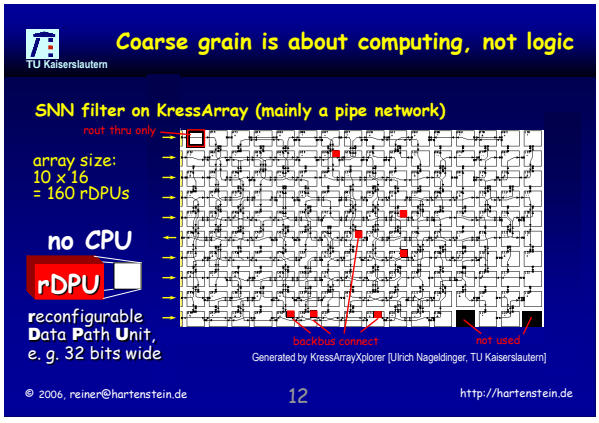
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Coarse grain is about computing, not logic
SNN filter on KressArray (mainly a pipe network)
rout thru only
array size:
10 x 16
= 160 rDPUs
no CPU
rDPU
reconfigurable
Data Path Unit,
e. g. 32 bits wide
backbus connect
not used
Generated by KressArrayXplorer [Ulrich Nageldinger, TU Kaiserslautern]
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The supercomputing paradigm trap

this did not prevent supercomputing from following the wrong rodmap for decades, imprisoned by the von Neumann paradigm trap

No technology transfer from Mathematics:
caught by the algebraic paradigm trap
(systolic array scene)

The language and tool disaster

End of April '06 a DARPA brainstorming conference:

Software people do not speak VHDL
Hardware people do not speak MPI
Bad quality of the application development tools

A poll at FCCM'98 revealed, that
86% of hardware designers hate their tools !!

Escaping the paradigm trap

The underground success story of FPGAs

Massive speed-up

Slashing the electricity bill

However, this is not supported by our education systems

Unqualified for RC ?

Using FPGAs for scientific computation?
hiring a student from the EE dept. ?

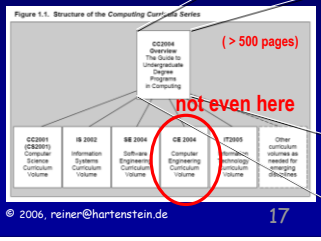
application disciplines use their own trick boxes:
transdisciplinary fragmentation of methodology

CS is responsible to provide a RC common model
- for transdisciplinary education
- and, to fix its intradisciplinary fragmentation

Curricula ?

(chair: Peter Denning) **Joint Task Force for Computing Curricula 2004 fully ignores Reconfigurable Computing**

FPGA & synonyma: 0 hits
(Google: 10 million hits)

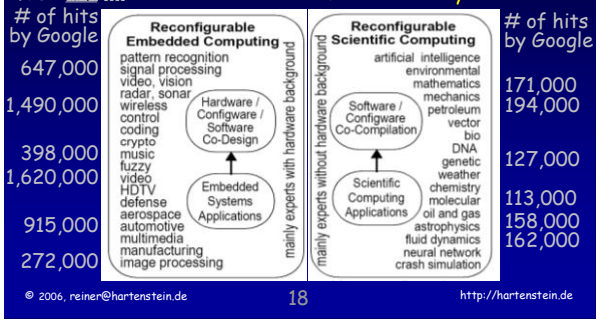


The Pervasiveness of RC

unqualified for RC ?

"FPGA **and** ...."

Math/SW-savvy scene



Curriculum Recommendations, v. 2005

Upon my complaints the only change: including to the last paragraph of the survey volume:

"programmable hardware (including FPGAs, PGAs, PALs, GALs, etc.)."

However, no structural changes at all

torpedoing the transdisciplinary responsibility of CS curricula

This is criminal !

Pervasiveness of FPGA application

More recently FPGAs as accelerators went also into every area of scientific computing

Compute-intensive: my talk does not really cover performance of bulk storage, discs, etc.

highlights the supercomputing paradigm trap and a fully ignored early solution

illustrates why behind FPGA success there is a hidden paradigm shift

What we learn for Low Power Design

Up to 4 orders of magnitude

For many published speed-up factors obtained from software-to-FPGA migration see Jürgen Beckers part of Monday tutorial

But before FPGAs came up, DPLA* (a programmable PLA) was successful inside the MoM colmputer architecture

*) designed at Kaiserslautern and fabricated via the German multi university E.I.S. project infrastructure

1986: Xputer Lab at Kaiserslautern: MoM I and II

The Reconfigurable Computing paradox

the effective integration density of FPGAs is behind the Gordon Moore curve by more than 4 orders of magnitude

- wiring overhead
- reconfigurability overhead
- routing congestion

- Low clock frequency
- Power-hungry
- Going worse for larger FPGAs

Remember: speed-ups up to 4 orders of magnitude

Reconfigurability per se is not the key

It's the paradigm shift coming along with it

Note: no instruction fetch at run time !

Data streams instead of instruction streams

Enabling technology for data sequencers (GAG) brings further performance improvements

A non-reconfigurable example is the BEE project (Bob Broderson et al., UC Berkeley)

Explanation of the RC paradox

Each technology providing a factor of 10 or more improvements over an established one, can be expected to become disruptive [Andy Grove].

The analysis of the Supercomputing crisis explains why the "bad" FPGA are so disruptive

49 firms failed [Gordon Bell, keynote at ISCA 2000: Dead Supercomputing Society, research 1985 - 1995]

Going toward "connected thinking"

[pwc.com]

The heyday of reductionism has passed.

Impenetrable obstacles have been encountered which cannot be solved by the classical simple reductionist approach.

"paradigm trap"

This is the reason of the growing worldwide significance of transdisciplinary notions

We need Coherence instead of fragmentation into specialists' niche areas

This is heralding a new era

Transdisciplinary Education?

Computer Science not prepared

Lacking **intra**disciplinary cohesion between the mind sets of:

- Theoreticians (Math background)
- Hardware People (edu)
  - Computer Architects
  - Embedded Syst. Designers
- Software People (Application Development)

for decades: the Hardware / Software chasm turns into: the Configware / Software chasm

FPGA use: A new direction in low power Design

PATMOS
http://www.patmos-conf.org
Grandfather of ISLPED
Sept. 13-15, 2006,
Montpellier,
France

as a panelist at:
2006 International Symposium on Low Power Electronics and Design, (ISLPED), October 4-6, 2006
Rottach-Egern, Tegernsee, Germany
http://www.islped.org/