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Reconfigurable Computing Architectures and Methodologies for System-on-Chip;
Reiner Hartenstein, Monday, November 19, 10:15 - 11:00 hrs.
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Configware / Flowware Compilation

high level source program

rewriter

intermediate

mapper

configured

scheduler

flowware

data sequencer

---

KressArray Family generic Fabrics: a few examples

Examples of 2nd Level Interconnect:
layouted over rDPU cell

- no separate routing areas!

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KressArray Xplorer

---

Without VHDL ....

Term Rewriting System (TRS):

- as a Module Generator Generator (TRS-MGG)
- Platform-based verification at very high level (math)

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Scalability for fine grain morphware

- FPGAs supporting CLB macro block cell concept
- Mapper using (macro) wiring by abutment
- Introduce new machine paradigm to undergraduate education
- Teach hardware / configware / software co-design

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Anti machine is the way to go
vN is obsolete for massive fine grain and coarse grain Morphware

Problems to be solved

• Microelectronics History
• fine grain and coarse grain Morphware
• Anti Matter of Computing
• Anti Machine and its Resources
• Problems to be solved

What is the trend?
• vN is needed for embedded systems, OS, compilers, Segekrantz software, non-performance-critical applications, others...
• vN is absolute for massive parallelism, except some special application areas
• Anti machine is the way to go for massive parallelism, also data-intensive applications
• Morphware is the way for high performance with short product life cycles, unstable standards

Conclusion: all knowledge needed is available

• machine paradigm
• languages
• hw/sw partitioning methodology
• compilation techniques
• anti architectural resources
• sequencing methodology: hw & sw
• parallel memory IP core and module generator vendors
• anything else needed

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Terminology: Digital System Platforms clearly distinguished

<table>
<thead>
<tr>
<th>platform</th>
<th>source running on it</th>
<th>machine paradigm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware</td>
<td>middleware</td>
<td>system paradigm</td>
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