# The „FIRSTs“ by the Xputer Lab

Reiner Hartenstein[1] (R. H.), TU Kaiserslautern, February 2015

**The Anti-Machine Paradigm (“Xputer”),** counterpart of the von Neumann paradigm by using data counters istead of a program counter [1]. Running data streams instead of instruction streams. To cope with the von Neumann Syndrome we urgently need this alternative machine paradigm. Data sequencers instead of an instruction sequencer: [2,3].

[1] N. N.: Xputer-related Literature; TU Kaiserslautern, 2015 <pdf>

[2] R. H.: Der Mikroprozessor im nächsten Jahrtausend; Elektronik 1/2000 <pdf>

[3] R. H.: High Performance Machine Paradigm based on Auto-sequencing Data Memory <pdf>

**Generalization of the Systolic Array** (“super-systolic array” or “Kress Array”) by introducing a new synthesis method and integrating auto-sequencing data memory (AsM) – adapting it into the Xputer paradigm

[ ] R. H., R. Kress: “A Datapath Synthesis System for the Reconfigurable Datapath Architecture”; Asia and South Pacific Design Automation Conference, ASP-DAC'95, Makuhari, Chiba, Japan, Aug./Sept. 1995 <pdf> <ppt>

[ ] R. H., M. Herz, Th. Hoffmann, U. Nageldinger: "KressArray Xplorer: A New CAD Environment to Optimize Reconfigurable Datapath Array Architectures"; The 5th Asia and South Pacific Design Automation Conf. ASP-DAC 2000, Pacifico Yokohama, Yokohama, Japan, Jan 25-28, 2000. <pdf>

[ ] R. H.: "Generalization of the Systolic Array"; memorandum, CSG, TU Kaiserslautern, Oct 2003, <pdf>

[ ] R. H.: “KressArray: what is the achievement ? Generalization of the Systolic Array”; memo, TU Kaiserslautern, 2013 - <pdf>

[ ] R. H: “Karl Steinbuch about how to invent something”; Memo, Nov. 2014 <pdf>

**A Data-procedural Programming Language.** In 1993 introucing the first data-procedural programming language (MoPL: Map-oriented Programming Language) supporting the Xputer machine paradigm (w. data couners instead of a program counter): to program data streams instead of instruction streams.

[ ] R. H., A. Ast, J. Becker, R. Kress, H. Reinig, K. Schmidt: “MoPL-3: A New High Level Xputer Programming Language”; submitted to 3rd International Workshop on Field Programmable Logic and Applications, Oxford, UK, Sept. 1993 <pdf>

[ ] R. H., A. Ast, J. Becker, R. Kress, H. Reinig, K. Schmidt: “Data-procedural Languages for FPL-based Machines”; 4th International Workshop on Field Programmable Logic and Application (FPL'94), Prague, Sep 7-10 1994, <pdf>

[1] Full Professor TU Kaiserslautern, Adjunct Profesor KIT Karlsruhe, IEEE life fellow, FPL fellow, SDPS fellow

## Reconfigurable Computing Compiler, ……

[ ] R. H.:

## FPGA usage for saving energy, ……

[ ] R. H. (keynote address): "Reconfigurable computing means to brave the paradigm chasm"; The HiPEAC Workshop on Reconfigurable Computing, Gent, Belgium, January 28, 2007 <pdf>

[ ] R. H.: "Are Supercomputers an Endangered Species? Computerized Infrastructures going to cause an Energy Crisis." <pdf>

[ ] R. H.: contribution to the panel entitled "Flexibility and Low Power; a Contradiction in Terms?" Peter Wintermayr, Editor in Chief of Markt & Technik (moderator), Reiner Hartenstein, TU Kaiserslautern; Heinrich Meyr, RWTH Aachen and CSO CoWare; and Steve Leibson, Tensilica; The 8th International Symposium on Low Power Electronics and Design 2006 (ISLPED), October 4 - 6, 2006, Tegernsee, Germany <pdf>

## Re-definition of low power design for HPC: a paradigm shift

[ ] R. H. (conference opening keynote): "The Re-definition of Low Power Design for HPC: a Paradigm Shift"; 21st Symp. on Microelectronic Technology and Devices (SBMICRO 2006), Aug 28 - Sep 1, 2006, Ouro Preto, MG, Brasil <pdf>
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## The Generic Address Generator (GAG); <Figure 1>

[ ] (invited paper): Michael Herz, Reiner Hartenstein, Miguel Miranda, Erik Brockmeyer, Francky Cathoor: Memory Addressing Organization for Stream-based Reconfigurable Computing; The 9th IEEE International Conference on Electronics, Circuits and Systems - ICECS 2002, September 15-18, 2002, Dubrovnik, Croatia <pdf>

[ ] R. H., A. G. Hirschbiel, M. Riedmüller, K. Schmidt, M. Weber: A High Performance Machine Paradigm Based on Auto-Sequencing Data Memory; HICSS-24, Hawaii Int'l Conf on Sysstem Sciences, Koloa, Hawaii, 1991 <pdf>

[ ] R. H., A. Hirschbiel, M. Weber: The Machine Paradigm of Xputers and its Application to Digital Signal Processing Acceleration; 1990 International Conf. on Parallel Processing (ICPP 90), August 1990, St. Charles, Illinois, USA, <pdf>

[ ] R. H., A. Hirschbiel, M.Weber: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware; CONPAR '90 - VAPP IV, Sep 1990, Zürich, Switzerland <pdf>

[ ] R. H. (invited presentation): Reconfigurable Computing Development -- Trends; Dot Wireless Inc., San Diego, CA, USA, 1999 <pdf>

## The Shuffle Sort Algorithm

[ ] R. H., K. Bastian, W. Nebel): „VLSI-Algorithmen: innovative Schaltungstechnik statt Software - SHUFFLE SORT: VLSI-Beispiel eines Sortierers"; Ges. f. Meß- und

Regelungstechnik: Tagung Mikroelektronik in der Automatisierungstechnik, Baden-Baden 1985; VDI-Bericht 550, Düsseldorf 1985

[ ] Martin Duhl: Die schrittweise Entwicklung und Beschreibung einer Shuffle-Sort-Array Schaltung in HYPERKARL aus der Algorithmischen Darstellung des BUBBLE-SORT-ALGORITHMUS, Projektarbeit, TU Kaiserslautern 1986

[ ] R. H.: "The Shuffle Sort Algorithm“; Memo, TU Kaiserslautern, Nov 2013 <pdf>

## KARL Hardware Description Language

[ ] R. H.: The world-wide dominant hardware description language throughout the 80ies; <html>

[ ] R. H.: The KARL System (Summary); <pdf>

[ ] R. H.: KARL Users; <html>

[ ] R. H.: 89 KARL Licensee Sites;

[ ] R. H.: KARL pages (a survey); <html>

## ABL Graphic Blockdiagram language, ……

[ ] R. H.: Description of wiring patterns;

[ ] R. H.: Domino notation; Wiki about domino notation;

## Introducing Mead-&-Conway to the continent (EurAsia)

[ ] R. H.: Das E.I.S.-Projekt und andere EDA-Ergebnisse; <html>

[ ] R. H.: The E.I.S. Project and other EDA Achievements; <html>

## Automatic VLSI Synthesis by Term Rewriting

[ ] R. H.: Automatic VLSI Synthesis by top-down Term Rewriting (TR); <html>;

The axioms; Multiplier bit generation; Description ot the multiplier;

## The world-wide first complete VLSI synthesis environment

[ ] R. H.: The CVT Software Package around KARL and ABL; <Fig.33>

## FFT on Xputer

[ ] R. H., A. Hirschbiel, M. Weber: The Machine Paradigm of Xputers and its Application to Digital Signal Processing Acceleration; 1990 International Conf. on Parallel Processing (ICPP 90), August 1990, St. Charles, Illinois, USA, <pdf>

[ ] R. H., A. Hirschbiel, M.Weber: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware; CONPAR '90 - VAPP IV, Sep 1990, Zürich, Switzerland <pdf>

## KressArray: the Generalization of the Systolic Array,

[ ] R. H.: Karl Steinbuch about how to invent something; <pdf>

**Founder of the first international conference series about energy-efficient computing**

[ ] R. H.: The PATMOS Page; <html>

[ ] R. H.: The History of the International Workshop on Power And Timing Modeling Optimization and Simulation (PATMOS); <html>

**karl-steinbuch**.org/
http://www.fpl.uni-kl.de/papers/publications/karl-steinbuch_en.html
http://www.fpl.uni-kl.de/papers/publications/karl-steinbuch.html

# Coined the Terms:

**Domino Notation,** ……

**Structured Hardware Design, Structured LSI Design**, ……

**Auto-sequencing Memory (AsM)** , ……

**Konferenz-Gründungen:**