Novel High Performance Machine Paradigms and Fast-Turnaround ASIC Design Methods: a Consequence of, and, a Challenge to, Field-programmable Logic

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Abstract. New high performance computational paradigms have been introduced, such as Xputers. Xputers have a reconfigurable ALU using FPGA-like technology. This results in an efficient novel machine paradigm, competitive to many ASIC solutions. It permits systematic derivation of machine code from high level algorithm specs or programs. After testing and debugging real gate array specs may be derived by retargeting. This is a shortcut on the way from algorithm to silicon: less effort and shorter time to market. Compared to conventional ASIC design this means: a) real execution instead of simulation, b) higher source language level and thus more concise specification.

1 Introduction

An increasing number of researchers uses field-programmable logic for more sophisticated concepts, than just ASIC prototyping: ASIC emulation [1, 2], simulation acceleration [3], customized (von Neumann) computers [4], a universal smart memory methodology [5]. This paper deals with FPL-based implementation concepts for Xputers. The Xputer paradigm is a high performance alternative to the von Neumann machine paradigm. All this work indicates an emerging completely new branch of computing science, where fundamental procedural models of universal computational paradigms are no more based on sequential program code, being scanned from a memory, but on structural programming [6].

Xputers have a reconfigurable ALU (called rALU), based on FPGA-like technology. Fig. 1 shows the basic structure of the rALU for the MoM-4 Xputer architecture [7]. This rALU includes a number of high performance operator resources (fig. 1: h-functors, where h stands for hardwired, such as ALUs, Multipliers etc.), a field-programmable logic part for residual control [8] and customized operators (f-functors, where f stands for field-programmable), as well as four scan caches (scan windows to scan primary memory space: size and dimension are adjustable at run time [9], currently up to 5 by 5 words, or 2 dimensions, respectively).

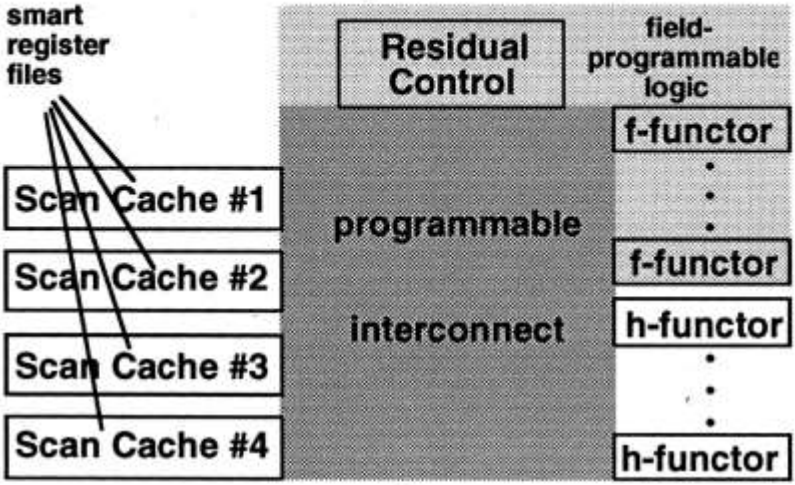

Fig. 1. rALU of the MoM-4

2 Reconfigurable Super ALU (rALU) for Acceleration

Such a rALU supports the configuration of one ore more powerful compound operators, which provide some intra-ALU parallelism (fig. 4 a) reducing the need to store and load intermediate values. A global interconnect-programmable part (see fig. 1) gives the flexibility needed to connect problem-oriented compound operators to the scan caches. In contrast to microprogrammable (e. g. von Neumann) ALUs, such compound operators are set up at loading time to avoid massive multiplexing overhead, addressing overhead, and control overhead [7, 9, 10]. The basic ideas for using such rALUs efficiently have been published elsewhere (such as: execution mechanisms [10], data-procedural programming languages and programming techniques [11, 12], compilation techniques [13], acceleration of applications in areas, such as image preprocessing [14], computer graphics [15], pattern recognition [16], digital signal processing [17], neural network emulation [18], VLSI design automation [19], and other areas [20]).

3 New Machine Paradigms Required for Structural Programming

The consequence of this is, that an Xputer does not have a hardwired instruction set, and, that an essential part of the machine code is combinational (fig. 2). That's why the rALU does not support any instruction sequencing (such as known from the von Neumann machine paradigm), so that another sequencing method is needed. That's why for Xputers data sequencing is used with a data counter (see fig. 2) - instead of the program counter known from von Neumann. Thus this creates the need for a fundamentally new basic computational model, i. e. for a completely new branch of computer science (see introduction). Figures 3 a and b illustrate the fundamental difference of

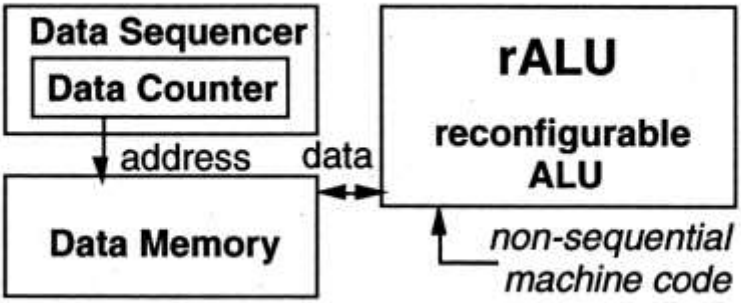

Fig. 2. Xputer Data Counter

the driving force: xputers are driven by data address sequences such, that control is a secondary level action to be evoked only upon request (fig. 3 b), in contrast to the (von Neumann) computer, driven by control flow (fig. 3 a), such, that data accesses are secondary actions, called from control flow. Sequencing within Xputers we call data sequencing (to distinguish this from the principles of so-called data flow machines, which in fact are driven by arbitration, or, by firing). The data-procedural implementation of an algorithm on an Xputer we sometimes call a data schedule for clear distinction from the familiar control-procedural von-Neumann-based implementations called programs.

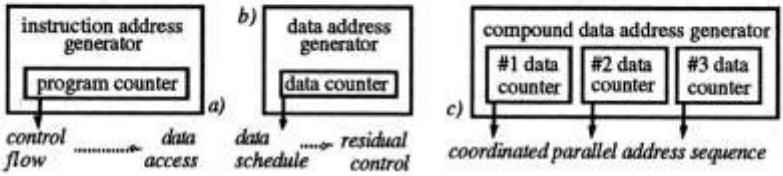

Fig. 3. Xputers vs. von-Neumann

4 The New Paradigm is much more Efficient

The data-procedural paradigm of Xputers efficiently supports much more efficient compilation techniques, than possible for (von Neumann) computers. The derivation of data sequences by data dependency analysis from high level algorithm specifications is more direct than generating control-driven conventional machine code. The machine code obtained by the new method is shorter and much less overhead-prone than von Neumann type machine code for a number of reasons explained elsewhere [19, 20]. That's why by this method highly efficient implementations can be achieved on a simple and cheap hardware. Often such solutions are competitive to ASIC solutions, although being based on a sequential paradigm. Acceleration factors (benchmark comparisons) by mostly two and up to three orders of magnitude have been obtained

experimentally for several example algorithm implementations on a monoprocessor MoM Xputer [22] (compared to technologically comparable von Neumann processors). These experiences indicate the feasibility of the following Xputer application scenarios: Xputers as universal accelerator co-processors on extension boards within workstations, and, the Xputer paradigm as basis of a more efficient new ASIC design method.

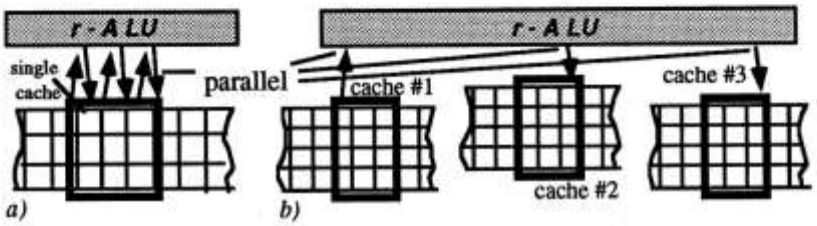

Fig. 4. Fine-Grain Parallelism Within the rALU

5 A Fast Turn-Around ASIC Design Method

This new ASIC design method is summarized by fig. 5, which is derived from am experimental environment having been implemented at Kaiserslautern [11]. An optimizer (a kind of program generator) accepts a high level specification and generates a program expressed in a high level programming language, from which the compiler generates "machine code" for a programmable version of an Xputer. Debugging turnaround is very fast, since real execution is used (instead of the highly inefficient simulation needed in other design environments). As soon as debugging is completed, a retargeting software will convert the machine code into a real (non-field-programmable) gate array design. Thus by retargeting a hard-coded hardwired version of the Xputer application is created. The compilation technique thus obtained is more than just silicon compilation. It starts with a more concise problem description input at a higher source language level, and, it generates target hardware, programs, and machine code at the same time, whereas silicon compilers only generate the target hardware. This new technique is also a new direction in high level synthesis.

6 The Super rALU is the Challenge

The extraordinarily good efficiency of the new paradigm and the surprisingly good performance figures obtained with it are highly promising. A challenge, however, because being a critical issue is the underlying field-programmable hardware technology. Especially the use of more than one scan cache [19] (fig. 3 c) in algorithms like FFT [10] creates a kind of parallelism (compare fig 4 b), where several register files communicate with each other through a common compound operator (on a kind of super rALU). For such an approach field-programmable circuits currently available commercially tend to yield extremely area-inefficient solutions. They mainly support glue logic solutions. That's why we need completely new approaches to the micro-

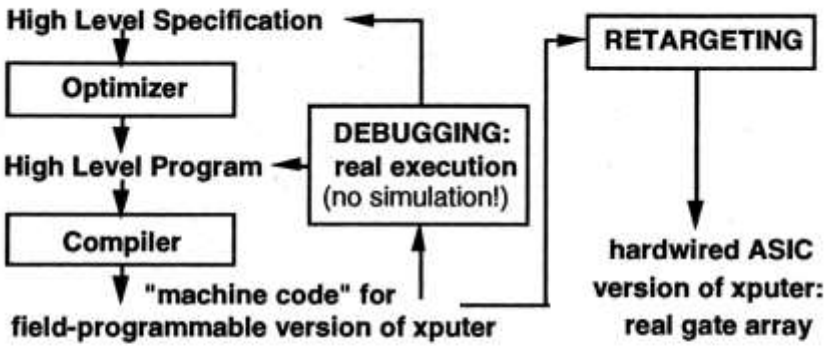

Fig. 5. New ASIC Design Method

architecture of field-programmable circuits. We need several different new micro-architectures of interconnect-reprogrammable ALUs, specialized for several application areas (digital signal processing, image processing, mathematics, high performance number crunching etc.). For some applications single-chip rALU solutions are feasible, such as e. g. for pattern matching [9, 14], where we designed our own field-programmable circuit (DPLA = Dynamically Programmable Logic Array, see fig. 6), since those available commercially did not meet out requirements. But for a high performance universal super rALU currently a MCM implementation would be needed.

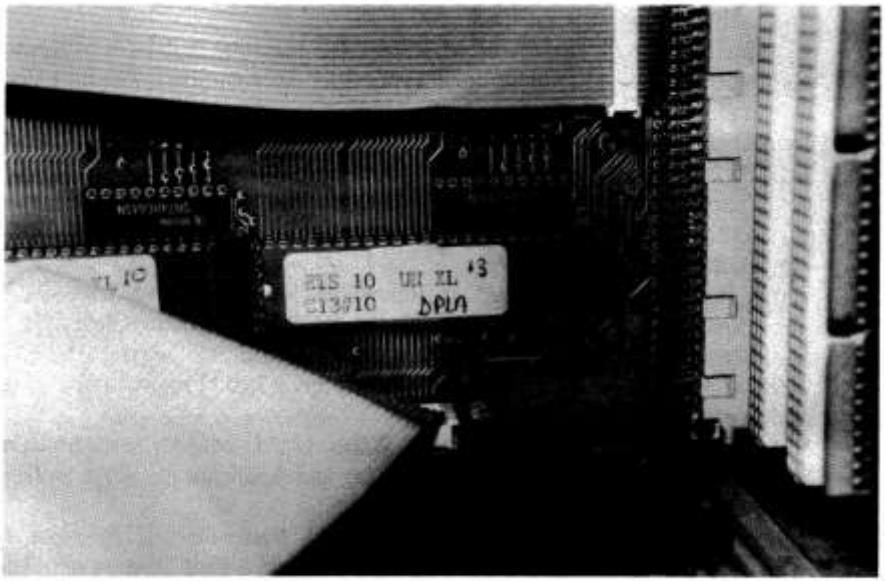

Fig. 6. A DPLA IC on the MoM rALU Board

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