(has been declined in 2005 by the IEEE-CS BoG pubs board)

or discussing other methods to extend the reach of IEEE Computer Society

Proposal of a new Magazine

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- DRAFT -

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Preface

During the past decade worldwide a huge new R&D and commercial scene with new markets has formed around an innovative basic computing paradigm: Reconfigurable Computing based on structurally programmable hardware platforms (which I would like to call „Morphware“ [TM[1]]). The size and high growth rate of this new scene is illustrated not only by a large number of new conferences with growing numbers of attendees as well as by the extended scope of many „traditional conferences“, pointing to this new scene. By the way: morphware is the fastest growing sector of the semiconductor market (currently approaching 6 Bio $).

A huge new commercial and R&D scene emerged around Reconfigurable Computing.

1. Trademark, DoD-funded morphware forum: http://www.morphware.org - (also see http://www.morphware.net)

Because I am intensively involved as a committee member of numerous conferences, and, as co-founder and multiple program chair, as well as multiple keynote or invited speaker of such conferences, I have the grip on a very large network of personal contacts to the key players worldwide. I would like to make this available for founding a profitable new journal. I am ready to serve and I have the time to do so.

A large network is available with personal contacts to the key players worldwide.

Fig. 1. illustrates the degree of penetration by the area already now. We should not hesitate to come up with the new journal, since we still have the chance to bring together an enormous number of subgroups by the proposed general journal (see Fig. 5.). Your may check quickly by yourself the pervasiveness of Reconfigurable Computing by using the automated search page **http://fpl.org/pervasiveness.html .** Fig. 1. shows a list of all the application areas for your easy googling by just clicking the keyword on this page.

If we do not hesitate, we still have the chance to become the only common voice of all these subgroups (also see Fig. 5.). We should not wait until some of these groups are beginning to found their own journals. Currently I am not aware of any subgroups planning such a periodical. However, North Holland /American Elsevier is planning a general journal on Reconfigurable Computing and related areas.

Reconfigurable Computing as „FPGA“: almost 10 million hits.

A good cooperation with the flagship magazine, e. g. by a special issue on Reconfigurable Computing, would be very helpful to provide a worldwide visible jump start for the proposed new journal. I would like to propose a special issue of the flagship magazine on Reconfigurable Computing education, also publishing carefully selected papers from the Reconfigurable Education Workshop at Karlsruhe, Germany, March 1, 2006

1 Introduction

The role of the proposed new journal. Magazines like Comm. ACM or IEEE COMPUTER could remain the flag ship journal, but should have a monthly Reconfigurable Computing column and should publish articles of common interest in Reconfigurable Computing. However, the total area of Reconfigurable Computing, Reconfigurable Logic, and all its application areas have grown by such an enormous extent (see below), that flagship magazines have by far not sufficient space available to cover even only a fraction of all important aspects. The number of application areas is still growing. More recently bio informatics, bio engineering, pharmaceutical computation, medical engineering, computational chemistry, computational physics, astrophysics, automotive, aerospace, military, and many other application areas have gone reconfigurable.

..found by Google

keyword	# of hits by Google (20. Jul. 06)
FPGA	9,960,000
Reconfigurable Computing	408,000
Configware	18,700
Anti Machine (different meanings)	18,800

Fig. 1. 10 million hits.

Check the pervasiveness of Reconfigurable Computing by <u>one click</u> per application area:

http://fpl.org/pervasiveness.html

Sure, You will be fascinated !

The Role of Accelerators. Hardwired accelerators, the result of software-to-hardware migration, are found everywhere for speed-up by avoiding the problems given by the sequential nature of instruction-stream-based traditional computing. For instance, a PC cannot maintain its own display without support by an accelerator (graphics chip or board). Because of skyrocketing mask cost, design cost, and design time, software-to-configware[1] migration for Reconfigurable Computing (RC) is a highly important alternative method, where similar speed-up factors can be obtained as known from hardwired accelerators. Compared to classical instruction-stream-based computing, such RC is based on a different common model and a fundamentally different mind set, which is often stalled by massive educational problems, even more drastic than by the well-known hardware / software chasm, the qualification problem in software-to-hardware migration. An important goal of the new journal is the break-through by solving these problems (section 1.2).

1.Configware, not instruction-stream-based, is the programming source for Reconfigurable Computing platforms.

(Structurally) Programmable Accelerators. RC means the replacement of hardwired accelerators by (structurally) programmable platforms, which migrates the definition of wiring patterns and operator specs from before fabrication to the customer's location after delivery.

Microelectronics Design Crisis. Programmable accelerators are a fundamentally different business model, also avoiding the very high mask cost and other NRE cost of specific silicon by using COTS[1] reconfigurable platforms. For RL vendors this has created an IC market volume of 3 billion US-Dollars, the fastest growing segment of the semiconductor market, predicted to grow to $5 billion by the year 2007[2].

The new journal: an excellent chance to win more members.

Going into Every Application Area. (Fig. 1.) Many years ago the use of reconfigurable platforms went from niche technology to mainstream. DaimlerChrysler, for instance, has a contract with Xilinx, the largest FPGA[3] vendor, for creating FPGA architectures for automotive applications. Los Alamos National Laboratory has developed a FPGA-based self-repairing computing system scheduled for being launched into orbit. Recently Cray has introduced a supercomputing module including a FPGA-based accelerator. MAPLD, a special conference serves the needs of NASA and military applications for reconfigurable platforms (see section 2.1). Fig. 5. lists much more very active application areas of reconfigurable platforms. Also the call for papers of many conferences (see chapter 2) list a wide variety of application areas.

… found by Google			
FPGA and ...	# of hits (Jan. 2006)	FPGA and ...	# of hits (Jan. 06)
... embedded	3,280,000	.... mathematics	171,000
... memory	2,370,000	..... fuzzy	167,000
.... computer	2,230,000	.... fluid dynamics	162,000
... control	1,690,000	.... astrophysics	158,000
.... performance	1,650,000	... acceleration	156,000
... video	1,620,000	... bio	140,400
... wireless	1,490,000	.... genetic	127,000
.... conference	1,090,000	.... sensing	121,000
... automotive	915,000	... weather	118,200
... multimedia	731,000	... chemistry	115,800
... manufacturing	715,000	... speed-up	115,000
... medical	710,000	... molecular	113,000
... high performance	706,000	.. computer architecture	113,000
.. signal processing	647,000	.... HDTV	107,000
.... virtual	594,000	.... mechanics	104,000
... low power	541,000	.... neural network	92,100
... VLSI	524,000	...artificial intelligence	89,500
... physics	508,000	.... DNA	87,200
... knowledge	415,000	.... pattern recognition	79,000
.... CAD	411,000	.. software defined radio	75,500
... music	398,000	.... crypto	70,600
.... vision	365,000	....computer graphics	66,200
.... coding	317,000	supercomputing	65,800
... defense	287,000	... HPC	57,400
... image processing	272,000	.... data mining	55,800
.... environmental	257,000	.... combustion	46,600
... chemical	247,000	.network architecture	38,800
..... vector	239,000	... black hole	30,000
... computational	238,000	... multi protocol	27,100
... intelligence	231,000	... petroleum	27,000
.... evolution	212,000	... oil and gas	22.300

Fig. 1. FPGAs going into every application area: hit rates growing.

The emerging Configware Industry. Using software is RAM-based, which is the secret of success of the software industry (and of the wealth of Bill Gates). The RAM provides the flexibility. Now we have a second RAM-based source: configware. Supporting reconfigurable computing and reconfigurable logic, an emerging configware industry is already growing. Not being instruction-stream-based, configware is fundamentally different from software. Configware engineering is the emerging counterpart of software engineering.

Reconfigurable Computing and computational biology make CS more fascinating, not only for students.

A highly promising Market for the proposed New Journal. Here is an urgent need and a rapidly upcoming large market for a new journal. Currently there is no other journal covering comprehensively RC, its impact on industry and academia, nor all other core issues related to it. The flagship magazines and a few other journals occasionally had a small section on RC, however, only inside single issues of these journals, but never regularly scheduled sections. Such efforts have covered only a very tiny share of the huge demand for publication by hundreds of researchers specialized in RC-related areas. Because of the different mind set existing journals usually hesitate to publish articles on these areas, also because the widely spread deficits in

1.COTS: Commodity Off The Shelf

2.Dataquest, June 2004

3. FPGA stands for „Field-Programmable Gate Array", a term, preferred by some FPGA vendors

a highly promising chance to make the journal profitable.

education affects the members of the editorial boards, as well as most reviewers. To an increasing extent partially RC-related articles appear in other journals covering application issues, rather than primarily covering the RC aspects. The flagship magazine does not have the space available to serve this huge market. The proposed new journal provides an excellent chance to win more members.

magazine brings new clientele to its publisher society: from biology, medecine, physics, chemistry, and many others.

Educational Deficits. Very often advances in Reconfigurable Computing and its application are torpedoed by educational deficits: the software / configware chasm, which, for instance, is a main reason of stalled progress in supercomputing by following the wrong road map for more than decade. Our CS curricula have mainly ignored the dominance of embedded systems coming along with the important role of reconfigurable accelerators (see Fig. 1.). There is a need for a new journal to attack these problem areas. Existing journals are no promising platforms for such challenges because of the „tunnel view“ perspective which stems from their traditional basic mind set. Reconfigurable Computing, i. e. using reconfigurable „hardware“ platforms like Reconfigurable Logic[1] (RL) integrated circuits (ICs) or coarse-grained reconfigurable platforms like Reconfigurable Data Path Arrays[2] (rDPAs), which, by the way, mean a generalization of systolic arrays, has become mainstream already years ago in embedded system development (digital signal processing, multimedia, wireless communication, encryption and other areas). More recently RL is also entering other areas like high performance computing (HPC), supercomputing (e. g. Cray), bio-informatics, molecular biology, chemistry and others.

1.1 Objectives and Perspectives of the New Journal

Its machine paradigm is the counterpart to the von Neumann paradigm and Configware Engineering is the direcft counterpart to Software Engineering, creating a strong trend toward dual-paradigm computing fundamentals. However, because of the configware / software chasm the dramatically growing Reconfigurable Computing publication activities are still mainly kept outside computing related journals, conferences and even curricula. It is the main goal of the proposed new journal to bridge the gap between these cultures and to present the extremly important new area for all members of the society publishing the magazine - instead of keeping it in a closed shop of a specialists' scene.

Why the topic areas are important. -Most software is embedded software, which doubles every 10 months (much faster than Moore's law). Reconfigurable Computing is an indispensable mainstream ingredient, not only in embedded systems. Its pervasiveness is overwhelming (Fig. 1.). It goes into every application area (Fig. 1.). It even goes to supercomputing.

Recent published activities in the area. -Section 2 of this poposal will cover the Growing Number of

Often tens of thousands or >100,000 hits by Google: search „FPGA + (one of the following keywords)“:

aerospace	**computer**	**fluid dynamics**	**mechanics**	**pattern recognition**
artificial intelligence	**computer architecture**	**geometric modeling**	**medical**	**physics**
astrophysics |	**computer graphics**	**high performance**	**mobile computing**	**robot**
automotive	**data mining**	**computing**	**molecular**	**supercomputing**
bio	**defense**	**HPC**	**n-body**	**virtual reality**
CAD/CAM	**EDA**	**image processing**	**network architecture**	**visualization**
chemical	**embedded systems**	**low power**	**numerical methods**	**VLSI**
combustion	**environmental**	**mathematics**	**oil and gas**	**wireless**

Fig. 1. The Pervasiveness of Reconfigurable Computing: auto-search @ **http://fpl.org/pervasiveness.html**

1.The „processors“ are one bit wide „configurable logic blocks“ (CLBs), embedded in reconfigurable interconnect fabrics.

2.Arrays of multiple bit wide RDPUs (Reconfigurable Data Path Units, with e. g. 32 bit or other word length).

Conferences dealing with Reconfigurable Computing. The list showing a total of 90 international conferences is far from being complete. The most impressive indication of the immense activities on more or less formal publication efforts are the numbers of hits found by Google (Fig. 1. and Fig. 1.).

Why the new journal is needed relative to other publications. -The machine paradigm of Reconfigurable Computing is the counterpart to the von Neumann paradigm and Configware Engineering is the direcft counterpart to Software Engineering, creating a strong trend toward dual-paradigm computing fundamentals. However, because of the configware / software chasm the dramatically growing Reconfigurable Computing publication activities are still mainly kept outside existing computing related journals, conferences and even curricula. Being guided by their von-Neumann-only mind set existing journals and magazines cannot bridge the configware / software chasm.

How to address the practical concerns of the publishing Society's readership. It is the main goal of the proposed new journal to bridge the gap between these cultures and to present the extremly important new area in a way accessible by all members. The dichotomy of the dual mind set philospohy needed for professional coverage can be provided only by the proposed new journal.

1.2 Important Missions of the proposed New Journal

Making CS more fascinating: also brings new members to ACM, or, IEEE Computer Society, rsp.

Ignoring the speed-up opportunities of Reconfigurable Computing is the reason of the stalled progress of supercomputing during more than a decade. Because reconfigurable computing does not need any instruction fetch during run time and massively reduces memory cycles needed for moving data around, this is the urgently needed way around the memory wall. It is unbelievable, that this important know-how has been ignored by this scene for such a long time, although this is based on loop transformations having been published by „classical" parallel computing scenes already in he 70ies and 80ies. Recently a minority of HPC and supercomputing scenes pays attention to the capabilities of reconfigurable computing. It should be a part of the important mission of the new journal to serve this growing minority.

Declining enrolment . at universities indicates that CS and related areas are going to be less attractive compared to biology and physics, and others. Young people, for instance, find molecular biology much more fascinating than CS and CS-related disciplines, which are boring, dominated by the more than 50 years old von Neumann paradigm indicating the mental monopoly of an instruction-stream-only basic mind set.

Making CS programs more fascinating. We should make CS more fascinating by introducing a dual-paradigm strategy: von Neumann, combined with a data-stream driven anti machine as a second basic paradigm to model Reconfigurable Computing. We should influence curriculum committees to update their proposals, already for freshmen level, maybe, even at colleges. It will be subject of the proposed new journal to provide the platform for hot discussions pushing into this direction.

Pushing Offshoring-resistant curricula. Also offshoring contributes to make CS appearing less promising. In fact, our current typical CS graduates are also not qualified for the labor market already now dominated by applications for embedded systems. It has been predicted[1], that by the year 2010 more than 90% of all applications programs will be implemented for embedded systems. Because of the mainly instruction-stream-based-only curricula our graduates are not qualified for software/configware/hardware partitioning decisions which are urgently required in developing contemporary and future embedded systems.

Google/Yahoo vs. ACM/IEEE recommendations		
key word	Google	ACM/IEEE curriculum[a] recommentations 2004
FPGA	9,960,000	0
reconfigurable	1,660,000	0
Reconfigurable Computing	296,000	0
reconfigurable logic	95,700	0
configware	13,400	0

a. search thru all documents by „find and replace" tool

Fig. 2. Ignorant curricula recommendations.

A huge number of conferences illustrates the immense size of the rapidly growing new area.

Reconfigurable platforms are meanwhile inevitable ingredients of embedded systems. However, typical CS graduates are not able to cope with systems including reconfigurable components or subsystems. So our students can acquire additional qualifications, currently not found in offshoring target countries. Although currently most graduates receive multiple job offers, these additional qualifications will be useful for any future developments.

Important Mission. It should be an important mission of the proposed new journal to lobby for fixing the current educational deficits in order to prepare our graduates for the already existing and rapidly growing segments of the labor market, and make them off-shoring-resistant by such upgraded qualifications.

key word	# of hits
FPGA & conference	1,090,000
FPGA & workshop (Oct. 2005)	328,000
FPGA & symposium	255,600
conference & "Reconfigurable Computing"	85,300
workshop & "Reconfigurable Computing"	52,200
symposium & "Reconfigurable Computing	46,300

Fig. 3. Conferences found by Google (20. Jan. 06)

URGENT. There are rumors, that North Holland / American Elsevier Publisher is working on coming up with a similar periodical. So, we should not hesitate in order to be at a top position of this promising new market - as soon as possible.

2 Growing Number of Conferences dealing with Reconfigurable Computing

The publication market growth in Reconfigurable Computing are also indicated by the rapidly growing number of conferences and the increasing attendance and number of submissions - of the RC area itself, as well as of other areas including RC-related subjects and aspects to their scope. Google hit rates (Fig. 1.) impressively illustrate the huge conference activity on Reconfigurable Computing and FPGAs. The categorized lists throughout this memo are very far from being a world-wide complete survey (compare no. of conferences found by Google: Fig. 3.)

Many direct international conferences of this area.

section	category of international conference series	listed
2.1	directly on Reconfigurable Computing	21
2.2	Biology-inspired Reconfigurable Computing	2
2.3	having RC as a main point of focus	57
2.4	having special tracks or keynotes on RC	33
2.5	RC in Supercomputing or Computer Conf'es	33
	total listed in this memo:	146

Fig. 4. The number of international conference series listed in this memo: it is very far from being complete.

2.1 Conferences directly on Reconfigurable Computing and related Areas

Starting in 1991 the number of international conferences on RC and related areas has been growing all the time: FPL, FPGA, FCCM, RAW, MAPLD, ERSA, where FPL is the oldest and largest international conference with almost 300 submissions and featuring 3 parallel session tracks throughout the conference (in 2004). Recently more conferences are coming up additionally: FPT (for Asia / South Pacific), RHPC, ARC, WARFP, as well as quite a number of local meetings not listed here, like, for instance, two meetings in Germany (about 70 attendees) in 2003 at DaimlerCrysler, Untertürkheim, and in 2004, organized by University of Paderborn.

FPL 2005 received 364 submissions.

The FPL annual Conference Series:

The International Conference on Field-programmable Logic, Reconfigurable Computing and Applications (FPL), http://fpl.org FPL is the oldest and largest international conference in the field, being hold annually in Europe: Oxford (UK), Vienna (Austria), Prague (Czechia), Darmstadt (Germany), London (UK), Tallinn (Estonia), Glasgow (UK), Villach (Austria); Montpellier (France), Lisbon (Portugal), Antwerp (Belgium),

1.British Department of Trade and Industry

Tampere (Finland). For its history also see: http://xputers.informatik.uni-kl.de/fpl/

The 16th International Conference on Field-programmable Logic, Reconfigurable Computing and Applications (FPL 2006) will be held end of August, 2005 at Madrid, Spain,

The 15th International Conference on Field-programmable Logic, Reconfigurable Computing and Applications (FPL 2005) has been held August 24 - 26, 2005 at Tampere, Finland, about 300 attendees http://fpl.org

The 14th International Conference on Field-programmable Logic, Reconfigurable Computing, and Applications (FPL 2004), Antwerp, Belgium, Aug. 30 - Sep 1, 2004; 3 parallel session tracks, 289 submissions, about 300 attendees

The 13th International Conference on Field-programmable Logic, Reconfigurable Computing, and Applications (FPL 2003), Sep 1 - 3, Lisbon, Portugal, about 250 submissions, about 270 attendees http://fpl.org

FPL		
year	submissions	attendees
2006	390	
2005	364	~300
2004	289	~300
2003	~250	~270

2nd - 12th FPL (FPL 1992-2002), Oxford (UK), Vienna (Austria), Oxford (UK), Prague (Czechia), Darmstadt (Germany), London (UK), Tallinn (Estonia), Glasgow (UK), Villach (Austria); Montpellier (France), http://fpl.org

The 1st International Conference on Field-programmable Logic, Reconfigurable Computing, and Applications (FPL 1991), Sep 4 - 6, 1991, Oxford, UK http://fpl.org

The FPGA annual Conference Series:

The ACM International Symposium on Field-Programmable Gate Arrays (FPGA): ACM/SIGDA, IEEE not involved

The 13th ACM International Symposium on Field-Programmable Gate Arrays (FPGA 2005[1]), Monterey, California. February 20-22, 2005, Monterey, California. http://isfpga.cs.caltech.edu/top.htm

The 12th ACM International Symposium on Field-Programmable Gate Arrays (FPGA 2004), Febr 22-24, 2004, Monterey, California. http://isfpga.cs.caltech.edu/www2004/index.htm

3rd - 11th ACM International Symposium on Field-Programmable Gate Arrays (FPGA 1995-2003), Monterey, CA

The 2nd ACM International Symposium on Field-Programmable Gate Arrays (FPGA 1994), Monterey, CA

The 1st ACM International Symposium on Field-Programmable Gate Arrays (FPGA 1993), Berkeley, CA

The FCCM annual Conference Series:

IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), http://www.fccm.org/

The 13th IEEE Symp. on Field-Programmable Custom Computing Machines (FCCM'05), April 2005, Napa, CA

The 12th IEEE Symp. on Field-Programmable Custom Computing Machines (FCCM'04), April 20-23, 2004, Napa, CA

The 11th IEEE Symp. on Field-Programmable Custom Computing Machines (FCCM'03), April 2003, Napa, CA

The 10th IEEE Symp. on Field-Programmable Custom Computing Machines (FCCM'02), April 2002, Napa, CA

The 9th IEEE Symp. on Field-Programmable Custom Computing Machines (FCCM'01), April 2001, Napa, CA

The 8th Annual IEEE Symposium on Field-Programmable Custom Computing Machines[2] (FCCM'00), Napa,

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1.Topic Areas (call for papers):

- **FPGA Architecture:** Novel logic block and routing architectures, combination of FPGA fabric and system blocks (processors, etc.), new commercial architectures, impact of modern and future technologies (including ultra-deep submicron and nanometer scale) on the design of FPGAs (e.g. soft errors, leakage, power density, fabrication defects).
- **CAD for FPGAs:** Placement, routing, logic optimization, technology mapping, system-level partitioning, logic generators, testing and verification, CAD for FPGA-based accelerators, CAD for incremental FPGA design.
- **Circuit Design for FPGAs:** Novel FPGA circuits and circuit-level techniques.
- **FPGA-based and FPGA-like computing engines:** Compiled accelerators, reconfigurable computing, adaptive computing devices, systems and software.
- **Rapid-prototyping:** Fast prototyping for system-level design, Multi-Chip Modules (MCMs), logic emulation.
- **Applications:** Innovative use of FPGAs, exploitation of FPGA features, novel circuits, high-performance and low-power/mission-critical applications, DSP techniques, uses of reconfiguration, FPGA-based cores.

2. FCCM **2000 top predictions** (by voting) for FCCMs in 2005

	comment by the year 2005:
A C derivative will be the dominant HDL. (7)	*not yet*
FPGA Systems-on-Chip are commonplace. (7)	*became true*
We will merely dislike the tools. (9) (See in previous years)	*no, tools still hated*
CPUs + FPGAs are a reality. (10)	*became true*
Still using VHDL (and hating it), still talking about C to Silicon. (10)	*still true*
Each FPGA has its own IP address. (15 votes)	*not yet*

California, April 2000

The 7th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'99), Napa, California, April 16 - April 18, 1999

The 6th Annual IEEE Symposium on Field-Programmable Custom Computing Machines[1] (FCCM'98), Napa, California, April 1998

The 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'97), Napa, California, April 16 - 18, 1997

The 4th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'96[2]), Napa, California, April 1996

1st - 3rd Annual Symp. on Field-Programmable Custom Computing Machines (FCCM'93-95), Napa, CA

FCCM		
year	submissions	attendees
2005		
2004	106	~143
2003	78	below (SARS..)
2002	73	~143
2001	57	
2000	67	

The RAW annual Workshop Series:

Reconfigurable Architectures Workshop - in conjunction with IPDPS[3]. - History: http://xputers.informatik.uni-kl.de/raw/index_raw.html#raw04

The 13th Reconfigurable Architectures Workshop (RAW 2006), April 26 - 27, 2006, at Rhodes Island, Greece

The 12th Reconfigurable Architectures Workshop (RAW 2005), April 4 - 5, 2005, Denver, Colorado

The 11th Reconfigurable Architectures Workshop (RAW 2004), April 26-27, 2004, Santa Fe, New Mexico, USA

1st - 10th Reconfigurable Architectures Workshop (RAW 1994 - 2003) at different places together with IPDPS.

RAW		
year	submissions	attendees
2005	58	~
2004	38	~
2003	47	~

The MAPLD annual Conference Series:

Military Application of Programmable Logic Devices

The 8th MAPLD International Conference, September 7-9, 2005, Ronald Reagan Building and International Trade Center, Washington, D.C. - hosted by the NASA Office of Logic Design.

The 7th MAPLD International Conference, September 8-10, 2004, Ronald Reagan Building and International Trade Center, Washington, D.C. - Over 130 Presentations: 35 Exhibitors

2nd - 6th MAPLD International Conference: 1999 - 2003

The 1st MAPLD International Conference: 1998

MAPLD				
year	submissions	presentations	attendees	exhibitors
2005	190			
2004	135	130	510	35
2003	125		417	
2002	70		247	
2001			216	
2000			195	
1999			185	
1998	50		172	

The FPT annual Conference Series:

The International Conference on Field-Programmable Technology

FPT 2005: the 3rd International Conf. on Field-Programmable Technology, National University of Singapore,

FPT		
year	submissions	attendees
2005	143	
2004	122	~100
2003		92
2002		>100

1. FCCM **1998 top predictions** (by voting) for FCCMs in 2003 — *comment by the year 2005:*
   - CAD will be the killer app for FCCM. (8 votes) — ?
   - At FCCM '03, Mark Shand will give a paper on interfacing to the Hubble Telescope using FCCMs. (11) — *:-)*
   - FPGAs in FCCMs will have hardwired functional units (ALU, FPU, MPY, PCI...). (12) — *became true*
   - 90% of embedded systems on a chip will contain FPGA logic for FCCM-type usage. (14) — *became true*
   - We will still hate the tools. (27 votes: two thirds!) — *still true*

2. FCCM **1996 top predictions** (by voting) for FCCMs in 2001 — *comment by the year 2005:*
   - FCCM apps will be downloaded from the Internet. — *became true*
   - FPGAs used in FCCMs will have embedded functional units. — *became true*
   - Dynamic FPGAs with on-chip DRAMs in FCCMs. — *became true*
   - FCCM languages will be Visual Verilog++tm, gcc, and Matlab. — *became true except Visual Verilog++*
   - $100M/year FCCM industry with two public companies. — *my estimation: the order of magnitude may be true (depends on definition of „FCCM industry“)*
   - FCCM '01 will have 1K attendees and a 100 vendor trade show. — *not true for FCCM, but became true and even exceeded by summing up all RC conferences per year still true. For the forthcoming FPL 2005 at Tampere, Finland (364 submissions), an attendance of 500 is a realistic estimation.*

3. International Parallel and Distributed Processing Symposium

Singapore, December 11-14, 2005

FPT 2004: the 3rd International Conf. on Field-Programmable Technology, Univ. of Queensland, Brisbane, Australia, Dec. 6 - 8, 2004, - 122 submissions, >100 attendees http://www.icfpt.org

FPT 2003: the 2nd IEEE International Conf.on Field-Programmable Technology, The University of Tokyo, JAPAN, December 15-17, 2003 - attendees: 92

FPT 2002: the 1st IEEE International Conference on Field-Programmable Technology, Hong Kong, December 2002, attendees: >100

International Workshop on Reconfigurable Computing Education (RC education)

The 1st International Workshop on Reconfigurable Computing Education (RC education 2005) will be held March 1, 2005 at Karlsruhe, Germany, in conjunction with the IEEE Computer Society Annual Symposium on VLSI, March 2–3, 2005, Karlsruhe, Germany. http://fpl.org/RCeducation/ There are plans, to have the 2nd workshop in 2007 run by the IEEE Computer Society

The International Symposium on the Future of Configurable Hardware

International Symposium on the Future of Configurable Hardware, Dec. 6, 2005, Gent, Belgium http://www.elis.ugent.be/FCH

HiPEAC Workshop on Reconfigurable Computing; January 28, 2007, Ghent, Belgium http://ce.et.tudelft.nl/HiPEACRC_WS/

SMART Workshop on Statistical and Machine learning approaches applied to ARchitectures and compilaTion; January 28, 2007, Ghent, Belgium http://www.hipeac.net/smart-workshop.html

The annual Workshop Series on Rapid Prototyping:

The 16th IEEE International Workshop on Rapid System Prototyping (RSP'2005), June 8-10, 2005, Montreal, Canada

The 15th IEEE International Workshop on Rapid System Prototyping (RSP'2004), June 28-30, 2004, Geneva, Switzerland

The 14th IEEE International Workshop on Rapid System Prototyping (RSP'2003), June 9-11, 2003, San Diego, USA

The 13th - 9th International Workshops on Rapid System Prototyping: RSP'2002: July 1-3, 2002, Darmstadt, Germany; RSP'2001: June 25-27, 2001, Monterey, California, USA; RSP'2000: June 21-23, 2000, Paris, France; RSP'99: June 14-16, 1999, Clearwater, Florida, USA; RSP'98[1]: June 3-5, 1998, Leuven, Belgium.

Rapid Prototyping		
year	submissions	attendees
2005	78	70
2004	66	~60
2003	66	~50
2002		

The annual ERSA Workshop Series:

Engineering Of Reconfigurable Systems And Algorithms (ERSA) http://www.scism.sbu.ac.uk/ERA/ersa.html -- part of the International MultiConference in Computer Science & Computer Engineering

ERSA'05, June 27-30, 2005, Las Vegas, Nevada, USA http://www.scism.lsbu.ac.uk/ERA/ersa05/ersa05.html
ERSA'04, June 21-24, 2004, Las Vegas, Nevada, USA http://www.scism.sbu.ac.uk/ERA/ersa04/ersa04.html
ERSA'03 June 23-26, 2003, Las Vegas, Nevada, USA http://www.scism.sbu.ac.uk/ERA/ersa03/ersa03.html
ERSA'02 June 24-27, 2002, Las Vegas, Nevada, USA http://www.scism.sbu.ac.uk/ERA/ersa02.html

Annual Southern Conference on Programmable Logic (SPL)

SPL 2006, 2nd Southern Conference on Programmable Logic, Mar del Plata, Argentinia, March 8 - 10, 2006 http://www.splconf.org

SPL 2005, 1st Southern Conference on Programmable Logic, Mar del Plata, Argentinia, March 9 - 11, 2005

PACT Workshop on Reconfigurable Computing:

PACT'98 Workshop on Reconfigurable Computing, Paris, October 1998, in conjunction with the International Conference on Parallel Architectures and Compilers

Workshop on Architecture Research using FPGA Platforms:

The 2nd Workshop on Architecture Research using FPGA Platforms (WARFP 2006), in conjunction with HPCA-12, Austin, Texas, February 12, 2006, http://cag.csail.mit.edu/warfp2006

The 1st Workshop on Architecture Research using FPGA Platforms (WARFP 2005[2]), in conjunction with HPCA-11, San Francisco, Sunday, February 13, 2005, http://cag.csail.mit.edu/warfp2005

1. Reiner Hartenstein was invited to give a keynote address

Conference on Reconfigurable Computing and FPGAs:

ReConFig		
year	submissions	attendees
2005		
2004	67	95
2003		

The 4th International Conference on Reconfigurable Computing and FPGAs (ReConFig'06), September 27-29, 2005, San Luis Potosi, Mexico

The 3rd International Conference on Reconfigurable Computing and FPGAs (ReConFig'05), September 28-30, 2005, Puebla City, Pue., Mexico

The 2st International Conference on Reconfigurable Computing and FPGAs (ReConFig'04), Sep 20-21, 2004, Colima, Mexico, 67 submissions, attendees: ~95

The 1st International Conference on Reconfigurable Computing and FPGAs (ReConFig'03), - September 8 - 9, 2003, Apizaco, Tlax., Mexico http://ccc.inaoep.mx/fpgacentral/reconfig04/

IEEE Workshop Heterogeneous reconfigurable Systems on Chip, Hamburg, April 2002.

Technical Symposium on Reconfigurable Computing with FPGAs, February 21-22, 2005, Manchester, UK http://www.csar.cfs.ac.uk/services/courses/fpga1.shtml

Reconfigurable Systems Summer Institute (RSSI), July 11-13, 2005, Urbana-Champaign, IL, USA http://www.ncsa.uiuc.edu/Conferences/RSSI/

The 1st Conference on Adaptive Hardware and Systems (AHS-2006), June 16- 18, 2006, Istanbul, Turkey http://ehw.jpl.nasa.gov/events/ahs2006/

The 2nd International Workshop on Reconfigurable Communication Centric System-on-Chips (ReCoSoC'06), July 3 - 5, 2006, Montpellier, France http://www.lirmm.fr/RECOSOC06/

2.2 Biology-inspired International Reconfigurable Computing Conferences[1]

NASA/DoD annual Conference on Evolvable Hardware (EH):

The 7th NASA/DoD Conference on Evolvable Hardware (EH-2005) June 29 - July 1, 2004 Washington DC, USA, http://ic.arc.nasa.gov/projects/eh2005/

The 6th NASA/DoD Conference on Evolvable Hardware (EH-2004) June 24-26, 2004 Seattle, Washington, USA, 99 attendees

The 5th NASA/DoD Workshop on Evolvable Hardware (EH-2003), Chicago, Illinois, USA, July 9-11, 2003, 100 attendees

The 4th NASA/DoD Workshop on Evolvable Hardware (EH-2002), Alexandria, Virginia, USA, July 15 - 18, 2002, 69 attendees

The 3rd NASA/DoD Workshop on Evolvable Hardware[2] (EH-2001), Long Beach, California, USA, July 12-14, 2001, 90 attendees

The 2nd NASA/DoD Workshop on Evolvable Hardware (EH-2000), Palo Alto, California, USA, July 13-15, 2000,- 95 attendees

The 1st NASA/DoD Workshop on Evolvable Hardware (EH-1999), Pasadena, California, USA, July 19 - 21, 1999, 111 attendees

EH		
year	submissions	attendees
2005		~100
2004		99
2003		100
2002		69
2001		90
2000		95
1999		111

The annual Conference on Evolvable Systems: from Biology to Hardware (ICES):

The 6th International Conference on Evolvable Systems, From Biology To Hardware (ICES'05), Barcelona, Spain, Sept. 12-14, 2005.

The 5th International Conference on Evolvable Systems: From Biology To Hardware (ICES2003), Trondheim, Norway, March 17 - 20, 2003

2.included in the list of topic areas:

- Languages and tools for rapid prototyping
- Memory system designs
- Multiprocessor designs on one FPGA
- Multiprocessor designs across multiple FPGAs
- System software support for FPGA prototypes

1.also see: http://xputers.ihttp://xputers.informatik.uni-kl.de/fpl/index_conf.html#evonformatik.uni-kl.de/fpl/index_conf.html#evo

2.subject areas:

- Evolutionary hardware design (including design of mechanical systems, electronic circuits synthesis)
- Real-world applications of evolvable hardware
- Co-evolution methods
- Online and offline evolution methods
- Hardware/software co-evolution
- Testbeds and evolutionary design automation tools
- Self-repairing hardware
- Self-reconfiguring hardware
- Embryonic hardware
- Morphogenesis
- Novel devices and hardware platforms suitable for evolution
- Adaptive hardware, adaptive computing
- Adaptive flight hardware

The 4th International Conference on Evolvable Systems: From Biology To Hardware (ICES2002)

The 3rd International Conference on Evolvable Systems: From Biology To Hardware (ICES2000)

The 2nd International Conference on Evolvable Systems: from Biology to Hardware (ICES98), Lausanne, Switzerland, September 23-26, 1998

ICES		
year	submissions	attendees
2005		
2004	70	75
2003		

The 1st International Conference on Evolvable Systems: from Biology to Hardware (ICES96), Tsukuba, Japan, October 7-8, 1996

(the 0th ICES) Towards Evolvable Hardware: An International Workshop, Lausanne, Switzerland, October 2-3, 1995, Lausanne, Switzerland, http://lslwww.epfl.ch/pages/events/seminar_09_95/home.html

2.3 RC as a Main Aspect in other Conferences

RC regularly appears as an experimental platform or as another main aspect to the subject of conferences like GECCO, CEC, EuroGP, SEAL, and many others. In this context sometimes the term „soft computing“ appears as a kind of synonym for RC. The list of conferences following below is far from being complete.

Annual International Symposium on Computer Architecture (ISCA):
The 33rd Annual International Symposium on Computer Architecture, June 17-21, 2006, Boston, MA, USA http://www.ece.neu.edu/conf/isca2006/

RC: main aspect in many other international conferences.

IEEE Custom Integrated Circuits Conference (CICC):
The 25th CICC, 2005: September 18 - 21, 2005, San Jose, California. http://www.ieee-cicc.org

DesignCon: DesignCon, Febr. 6-9, 2006, Santa Clara, CA, USA, http://www.designcon.com/

DesignConEast:
DesignConEast, Sept 19-21, 2005, Worcester, Mass, USA, http://www.iec.org/events/2005/designcon_east/

EuroDesignCon:
EuroDesignCon, Oct. 24-27, 2005, Munich, Germany, http://www.iec.org/events/2005/euro_designcon/

International Conference on Information Technology: New Generations (ITNG)
ITNG 2006: Third International Conference on Information Technology : New Generations; April 10-12, 2006, Las Vegas, Nevada, USA http://www.itng.info 4th: April 2-4, 2007 Las Vegas, Nevada, USA

The 49th IEEE International Midwest Symposium on Circuits and Systems
(MWSCAS), August 6 - 9, 2006, San Juan, Puerto Rico, USA http://mwscas06.uprm.edu/call4papers.html

9th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems
(DDECS), April 18-21, 2006, Prague, Czech Republic http://ddecs06.felk.cvut.cz/

System Level Interconnect Prediction (SLIP)
SLIP 2003, Monterey, CA, USA, April 5-6, 2003; SLIP 2004, Paris, France, February 14-15, 2004; SLIP 2005, San Francisco, CA, USA, April 2-3, 2005; SLIP 2006, March 4-5, 2006, Munich, Germany http://sliponline.org/

Workshop on Application Specific Processors (WASP):
WASP 2005: The 4th Workshop on Application Specific Processors, September 22, 2005, New York Metropolitan Area, USA - http://dogbert.eng.umd.edu/wasp05/index.html
WASP 2004: The 3rd Workshop on Application Specific Processors, September 7, 2004, Stockholm, Sweden
WASP 2003: The 2nd Workshop on Application Specific Processors, December 2, 2003, an Diego, CA, USA
WASP 2002: The 1st Workshop on Application Specific Processors, November 19th, 2002 in Istanbul, Turkey
The call for papers of WASP2005, for instance, includes the following RC-relevant topic areas: (Re)configurable processor architectures, Dynamically reconfigurable processors (Microarchitectural, Coarse-grained, FPGA, etc.), Compiler techniques for processor customizations, and, OS and Middleware support for application-specific processors. Remark: also the programming of reconfigurable platforms usually means application-specific instantiations of customization.

International Conference on High Performance Embedded Architectures & Compilers

HiPEAC 2007: 2007 International Conference on High Performance Embedded Architectures & Compilers, Ghent, Belgium, January 29-30, 2007 http://www.hipeac.net/conference/

HiPEAC 2005: 2005 International Conference on High Performance Embedded Architectures & Compilers, Barcelona, Spain, November 17-18, 2005 http://www.hipeac.net/hipeac/hipeac2005/

International Conference on Embedded And Ubiquitous Computing (EUC)

EUC'2006 - The 2006 IFIP International Conference on Embedded And Ubiquitous Computing, August 01-04, 2006, Seoul, Korea, official topic area: Reconfigurable Computing; http://euc.wonkwang.ac.kr/

EUC'2005 - The 2005 IFIP International Conference on Embedded And Ubiquitous Computing, December 6 - 9, 2005, Nagasaki, Japan, official topic area: Reconfigurable Computing; http://euc05.euc-conference.org/

EUC'2004 - The 2004 IFIP International Conference on Embedded And Ubiquitous Computing, August 25 - 27, 2004, Aizu, Japan, official topic area: Reconfigurable Computing; http://oscar.u-aizu.ac.jp/EUC2004/

European Conference on Genetic Programming (EuroGP):

EuroGP2006: The 9th ....., 10-12 April 2006, Budapest, Hungary http://evonet.lri.fr/eurogp2006/
EuroGP2005: The 8th European Conference on Genetic Programming, 30 March - 1 April 2005, Lausanne,
EuroGP2004: The 7th European Conference on Genetic Programming, 5-7 April 2004, Coimbra, Portugal
EuroGP2003: The 6th European Conference on Genetic Programming, April 14 - 16, 2003, Essex, UK
EuroGP2002: The 5th European Conference on Genetic Programming, Kinsale, Ireland, April 3-5, 2002
EuroGP2001: The 4th European Conference on Genetic Programming, Lake Como, Italy
EuroGP2000: The 3rd European Conference on Genetic Programming, Edinburgh, UK, April 15-16, 2000; /
EuroGP1998: The 1st European Conference on Genetic Programming, Paris, France.

The annual Genetic Evolutionary Computation Conference (GECCO):

The 10th Genetic Evolutionary Computation Conference (GECCO 2006), Seattle, WA, July 8 - 12, 2006
The 9th Genetic Evolutionary Computation Conference[1] (GECCO 2005), Washington DC, June 25–29, 2005
The 8th Genetic Evolutionary Computation Conference (GECCO 2004), Seattle, WA, June 26-30, 2004.
The 7th Genetic Evolutionary Computation Conference (GECCO 2003), Chicago, Illinois, July 12-16, 2003
The 6th Genetic Evolutionary Computation Conference (GECCO-2002), New York City, July 9-13, 2002
The 5th Genetic Evolutionary Computation Conference (GECCO-2001), San Francisco, CA, USA, July, 2001.
The 4th Genetic Evolutionary Computation Conference (GECCO-2000), Las Vegas, NV, USA, July 8-12, 2000
The 3rd Genetic Evolutionary Computation Conference (GECCO-1999), Orlando, Florida, July 13-17, 1999
The 2nd Genetic Evolutionary Computation Conference (GECCO-1998), San Francisco, CA, USA, 1998

The annual IEEE Congress on Evolutionary Computation (CEC):

Sept 2-5, 2005, Edinburgh, UK, http://www.dcs.ex.ac.uk/~dwcorne/cec2005/
June 20-23, 2004, Portland, Oregon; December 8 - 12, 2003, Canberra, Australia; May 27-30, 2001, Seoul, Korea; July 16-19, 2000, San Diego, USA; July 6 - 9, 1999, Washington D.C., U.S.A

The annual European Workshop on Evolutionary Bioinformatics (EvoBIO):

Emphasis on algorithms based on evolutionary computation, neural networks and other novel optimization methods

4th EvoBIO: 10-12 April 2006, Budapest, Hungary http://evonet.lri.fr/eurogp2006/
3rd European Workshop on Evolutionary Bioinformatics, 30 March - 1 April 2005, Lausanne, Switzerland
2nd European Workshop on Evolutionary Bioinformatics, 5-7 April 2004, Coimbra, Portugal
1st European Workshop on Evolutionary Bioinformatics, 14-16 April 2003, Essex, UK

The annual European Workshop on Evolutionary Computation in Hardware Optimization (EvoHOT):

Topics: evolvable hardware and problems such as routing, placement, or test pattern generation

3rd EvoHOT: 10-12 April 2006, Budapest, Hungary http://evonet.lri.fr/eurogp2006/
2nd EvoHOT: 30 March - 1 April 2005, Lausanne, Switzerland
1st European Workshop on Evolutionary Computation in Hardware Optimization, 5-7 April 2004, Coimbra, Portugal

The bi-annual Asia-Pacific Conference on Simulated Evolution And Learning (SEAL):

The 5th International Conference on Simulated Evolution And Learning (SEAL'04), Oct 26–29, 2004, Busan, Korea
The 4th Asia-Pacific Conference on Simulated Evolution And Learning (SEAL'02), Nov 18-22, 2002, Singapore

The bi-annual Conference on Artificial Evolution (AE):

The 7th International Conference on Artificial Evolution (AE-05), October 26-28 2005, Lille, France,
The 6th International Conference on Artificial Evolution (AE-03), October 27 - 30, 2003, Marseilles, France

1.Topic areas:

Genetic Programming	Evolutionary Programming	Evolvable Hardware	A-Life, Adaptive Behavior,	Evolutionary Scheduling and Routing
Genetic Algorithms	Real World Applications	Biological Applications	Agents, & Ant Colony Opt.	Search Based Software Engineering
Evolution Strategies	Learning Classifier Systems		Evolutionary Robotics	

Special tracks: many major international conferences.

The 5th International Conference on Artificial Evolution (AE-01), October 29-31, 2001, Le Creusot, France
The 4th International Conference on Artificial Evolution (AE-99), Nov. 3-5, 1999, Dunkerque, France.
The 3rd European Conference on Artificial Evolution (AE-97), Nimes, Oct. 1997
The 2nd European Conference on Artificial Evolution (AE-96), Heidelberg, Germany, September 1996.
The 1st European Conference on Artificial Evolution (AE-95), 1995, Brest, France,

Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI)
The 13th Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2006), April 3 - 4, 2006, Nagoya, Japan http://www.sasimi.jp/

European Conference on Machine Learning (ECML):
14th: ECML 2005, Oct 3 - 7, 2005, Porto, Portugal http://ecmlpkdd05.liacc.up.pt/
ECML 2004, Sept 20 - 24, 2004, Pisa, Italy http://ecmlpkdd.isti.cnr.it/
CML 2003, Sept 22 - 26, Cavtat-Dubrovnik, Croatia http://www.cs.kuleuven.ac.be/conference/ecmlpkdd/
13th: ECML 2002 Aug 19 - 24, 2002, Helsinki, Finland http://ecmlpkdd.cs.helsinki.fi/cfwt.html

International Conference on Evolutionary Programming (EP):
7th International Conference on Evolutionary Programming (EP98), Heidelberg, Germany, March 1998

The annual European Symposium on Intelligent Technologies, Hybrid Systems and their Implementation in Smart Adaptive Systems (EUNITE):
10 - 12 June 2004, Aachen, Germany http://www.eunite.org/eunite/events/eunite2004/eunite2004.htm
10 - 12 July 2003, Oulu, Finland http://www.eunite.org/eunite/events/eunite2003/eunite2003.htm
19 - 21 Sept 2002, Algarve, Portugal http://www.eunite.org/eunite/events/eunite2002/eunite2002.htm

The annual European Conference on Evolutionary Methods for Design, Optimization and Control with Applications to Industrial Problems (EUROGEN):
Sep 12 - 14 2005, Munich, Germany http://www.lhm.mw.tu-muenchen.de/EUROGEN05/EUROGEN05.pdf
Sep 15 - 17 2003, Barcelona, Spain http://congress.cimne.upc.es/eurogen03/frontal/default.asp
Sep 19 - 21 2001, Athens, Greece http://www.mech.ntua.gr/~eurogen2001

The bi-annual Conference on Adaptive Computing in Design and Manufacture (ACDM):
6th: ACDM2004, April 20 - 22, 2004, Bristol, UK http://www.ad-comtech.co.uk/ACDM2004.htm
5th: ACDM 2002, April 16 - 18, 2002, Exeter, Devon, UK http://www.ad-comtech.co.uk/ACDM2002.htm
4th: ACDM 2000, April 26 - 26, 2000, Plymouth, UK,
3rd: ACDM-1998, April 21 - 23, 1998, Totnes, Devon, UK

European Workshop on Evolutionary Robotics (EvoRobot):
EVOROBOT 2000, Third European Workshop on Evolutionary Robotics, April 17 -19, 2000, Edinburgh, UK
EVOROBOT 1998, First European Workshop on Evolutionary Robotics, April 1998, Paris, France

Other Conferences on Evolutionary Computation:

ICGA: International Conference on Genetic Algorithms

GP: 10th annual Genetic Programming Conference, Washington, DC, USA, June 25–29, 2005

CEC: 12th IEEE Congress on Evolutionary Computation, Edinburgh, UK, September 2 - 5, 2005

FOGA: Foundations of Genetic Algorithms

PPSN: Parallel Problem Solving from Nature

IEEE Conference on Evolutionary Computation

Alife: International Conference on Artificial Life

ECAL: European Conference on Artificial Life

ECML: European Conference on Machine Learning

AROB: 10th International Conference on Artificial Life and Robotics, Oita, Japan, Feb. 4-6, 2005.

ICANNGA: International Conference on Artificial Neural Networks and Genetic Algorithms

SAB: International Conference on Simulation of Adaptive Behavior

IASC: First International ICSC Symposium on Industrial Application of Soft Computing, Istanbul, Turkey, December 15 - 17, 2005

More recently most supercomputing conferences adopt this new area.

ISQED: IEEE 7th International Symposium on Quality Electronic Design, March 27-29, 2006. San Jose, CA, USA http://www.isqed.org

MICRO-38: The 38th Annual IEEE/ACM International Symposium on Microarchitecture, November 12-16, 2005, Barcelona, Spain http://pcsostres.ac.upc.edu/micro38/

IFMIP 2006 - 5th International Forum on Multimedia and Image Processing, July 25-28, 2006, Budapest, Hungary: Special Sessions on Information Security and Hardware Implementations.

IINC 2005 - IMAPS India National Conference (IINC) on Microelectronics & VLSI, Dec. 19-21, 2005, Mumbai, India - http://www.ee.iitb.ac.in/~imaps/index.htm

ITSW 2006 - 13th International Test Synthesis Workshop, April 9-12, 2006, Santa Barbara, CA, USA http://www.tttc-itsw.org/

ART-C - Workshop on Architectures for Real-Time Computing, December 5, 2004, Portland, OR, USA, http://www.cesr.ncsu.edu/artc

ESA - The 2006 International Conference on Embedded Systems and Applications (ESA-06), June 26-29, 2006, Las Vegas, Nevada, USA, http://juliet.stfx.ca/people/fac/lyang/esa-04/cfp.html http://juliet.stfx.ca/~lyang/esa-05/ http://www.world-academy-of-science.org/worldcomp06/ws/ESA/index_html

PDPTA- The 2006 International Conference on Parallel and Distributed Processing Techniques and Applications, June 26-29, 2006, Las Vegas, Nevada, USA http://www.world-academy-of-science.org/worldcomp06/ws/PDPTA/index_html

ICWN - The 2006 International Conference on Wireless Networks, June 26-29, 2006, Las Vegas, Nevada, USA http://www.world-academy-of-science.org/worldcomp06/ws/ICWN/index_html

ESC-China - The 6th Embedded Systems Conference - China, April 4-5, Shenzhen, PR China April 8-9, 2006, Beijing, PR China, April 12-14, Shanghai, PR China http://www.esconline.com/asia/

ESC-Taiwan 2006 - The 6th Annual Embedded Systems Conference-Taiwan, August 17-18, 2006, Taipei, Taiwan, http://www.esconline.com/asia/

ESC Silicon Valley - Embedded Systems Conference Silicon Valley, April 3 - 7, 2006, San Jose, CA, USA http://www.embedded.com/esc/sv/

ISLPED'06 - International Symposium On Low Power Electronics And Design, Oct. 4-6, 2006, Tegernsee (Munich area), Germany http://www.islped.org

WCNC 2006 - IEEE Wireless Communications and Networking Conference, 3 - 6 April 2006, Las Vegas, NV, USA http://www.ieee-wcnc.org/

9th Fuzzy Days - International Conference on Computational Intelligence; Sept. 18 - 20, 2006, Dortmund, Germany http://fuzzydays.cs.uni-dortmund.de/cfp.html

ASAP 2006 - IEEE 17th International Conference on Application-specific Systems, Architectures and Processors, September 11-13, 2006, Steamboat Springs, Colorado, http://asap2006.grm.polymtl.ca/

The 19th Symposium on Integrated Circuits and Systems Design (SBCCI2006), August 28 - September 1, 2006, Ouro Preto, Minas Gerais, Brasil http://www.sbc.org.br/sbcci

ICCAD - Int'l Conf. on Computer-Aided Design, Nov. 2 - 9, 2006, San Jose, CA http://www.iccad.com/cfp06.html

2.4 Special RC Tracks and/or Keynotes in other Conferences

A growing number of other international conferences includes RC and related topic areas in their call for papers, have major tracks specialized on RC, and/or invite speakers from the RC scene to give invited presentations or keynote addresses. Examples are also the huge conferences with thousands of attendees and also including large exhibits:

- the annual Design Automation Conference (DAC), held in the US http://dac.com
- the annual Conference on Design and Test in Europe (DATE) http://date-conference.com
- the annual EUROMICRO Conference On Digital System Design (DSD 2006) http://www.dsdconf.org/
- the annual Asia / Pacific Design Automation Conference (ASP-DAC) http://aspdac.com
- the IEEE International Conference on Computer Design (ICCD), http://www.iccd-conference.org
- the IEEE International Conference on Electronics, Circuits and Systems (ICECS)[1], http://www.icecs2005.rnrt.tn
- the IEEE/ACM/IFIP International Conference on Hardware - Software Codesign and System Synthesis (CODES+ISSS), http://www.codes-isss.org/
- the European Solid-State Device Research Conference (ESSDERC) and European Solid-State Circuits Conference (ESSCIRC) Series, http://www.esscirc.org/
- the World Congress on Lateral Computing (WCLC), http://www.lateral-computing.org/wclc/

1. For instance ICECS 2002, 9th IEEE International Conference on Electronics, Circuits and Systems, Dobrovnik, Croatia, had a special session on Reconfigurable Computing (organized by Reiner Hartenstein on invitation) - http://www.icecs2002.org/

- Annual ACM International Conference on Computing Frontiers (CF)[1] http://www.computingfrontiers.org
- the New EXploratory Technology (NEXT) Conference, http://next.utu.fi
- Annual Workshop on High Performance Embedded Computing (HPEC) http://www.ll.mit.edu/HPEC/hpec_03/
- International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES), http://www.casesconference.org
- 19th International Conference on VLSI Design / 3th International Conference on Embedded Systems, January 3 - 7, 2006, Hyderabad, India: FPGA-based design, Reconfigurable hardware design http://www.vlsiconference.com/
- IEEE World Congress on Computational Intelligence, July 16 - 31, 2006, Vancouver, Canada http://www.2006.org/
- IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips IX), April 19 - 21, 2006, Yokohama, Japan http://www.coolchips.org/
- HOT CHIPS 17 - A Symposium on High Performance Chips, August 14 - 16, 2005, Stanford University http://www.hotchips.org/hc17/program/program_at_a_glance.htm
- Bioinformatics Conference, August 11 - 14, 2003, Stanford University http://conferences.computer.org/bioinformatics/CSB2003/SectB.html
- ASPLOS-VIII - Eighth International Conference on Architectural Support for Programming Languages and Operating Systems, October 4-7, 1998, San Jose, California, http://arch.cs.ucdavis.edu/ASPLOS98/
- ECBS - 12th Annual IEEE International Conference and Workshop on the Engineering of Computer Based Systems, April 4 - 8, 2005, Greenbelt, MD, USA (Washington DC metro) http://abe.eng.uts.edu.au/ECBS2005
- SEW-29 - 29th Annual IEEE/NASA Software Engineering Workshop April 6 - 7, 2005, Greenbelt, MD, USA http://sel.gsfc.nasa.gov/website/29ieee.htm
- PASA - 8th Workshop in Parallel Systems and Algorithms, March 16, 2005, Frankfurt, Germany http:// www.iti.uni-luebeck.de/GI/PASA2006
- GLSVLSI 2006, April 30, 2006 –May 2, 2006, Philadelphia, Pennsylvania http://www.glsvlsi.org/

2nd Workshop on Unique Chips and Systems (UCAS-2) - in conj. w. IEEE Int'l Symposium on Performance Analysis of Systems and Software (ISPASS06) March 19, 2006, Austin, Texas http://www.ispass.org/ucas2/

WASA'06 - The International Conference on Wireless Algorithms, Systems, and Applications, August 15 -18, 2006, Xi'an, China http://wasa.cybersphere.net/

EC-06 - The 3rd International Workshop on Embedded Computing, August 14, 2006, Columbus, Ohio, USA, http://juliet.stfx.ca/~lyang/icpp06-ec/

SAMOS VI - Embedded Computer Systems:Architectures, MOdeling, and Simulation, July 17-20, 2006,Samos, Greece, http://samos.et.tudelft.nl/samos_vi/

DASS´2006 - Dresdner Arbeitstagung Schaltungs- und Systementwurf, May10 - 11, 2006, Dresden, Germany http://www.eas.iis.fhg.de/events/workshops/dass/2006/

WCAE 2006 - Workshop On Computer Architecture Education (in conjunction with the 33nd Int'l Symp. on Computer Architecture) June 17 or 18, Boston, MA, USA http://www4.ncsu.edu/~efg/wcae2006.html

IESS 2007 - International Embedded Systems Symposium, May 29 - June 1, 2007, Irvine, CA http://iess.org/

ESweek 2006 - Embedded Systems Week, Oct 22-27, 2006, Soelu, Korea http://esweek.org/

2.5 RC in Supercomputing Conferences and other CS conferences

A rapidly growing number of conferences on high performance computing, supercomputing and many other CS conferences adopt Reconfigurable Computing and related areas - not only just as an additional topic officially listed in the call for papers, but also emphasize a major focus on these areas. Examples are the following conferences and workshops.es

Workshop on Reconfigurable High Performance Computing[2]:

The 1st Workshop on Reconfigurable Systems for HPC (RHPC), held in conjunction with the Conference on High Performance Computing in Asia (HPC Asia 2004), July 21, 2004, Omiya Sonic City, Tokyo area, Japan - workshop attendees: about 50 - http://www.slrc.kyushu-u.ac.jp/~rhpc/

RHPC		
year	submissions	attendees
2005	~ 30	~50
2004		

Workshop on High Performance Reconfigurable Computing[3]

August 22 - 23, 2005,

1.annual conference, usually at Ischia, Italy (by ACM SIGMICRO, the 3rd one in May, 3-5, 2006), topic areas include: Non-conventional computing, Next generation high performance computing, Reconfigurable computing, Special purpose architectures, Compilers and operating systems, Supercomputing, SOC architectures, High performance embedded architectures, Computational intelligence frontiers: theory and industrial applications,Computational biology, and other topic areas

2. Reiner Hartenstein was invited to open this new workshop series by a keynote address.

Fairbanks, AK, USA, followed by a tutorial workshop on August 24[1] http://www.arsc.edu/news/FPGA.html

Workshop on Applied Reconfigurable Computing:

The 1st International Workshop on Applied Reconfigurable Computing (ARC 2005), Algarve, Portugal, February 22, 2005, http://w3.ualg.pt/~jmcardo/arc2005

The 2nd International Workshop on Applied Reconfigurable Computing (ARC 2006), Delft, The Netherlands, March 1-3, 2006 - http://www.arc-workshop.org/arc2006/

The 3rd International Workshop on Applied Reconfigurable Computing (ARC 2007), Mangaritiba, Rio de Janeiro, Brasil, March 27 - 29, 2007 - http://www.icmc.usp.br/~lcr/arc2007/

RMRC Regional meeting on Reconfigurable Computing; Mangaritiba, Rio de Janeiro, Brasil, March 26, 2007 - http://www.icmc.usp.br/~lcr/mrmc2007

SC Supercomputing:

SC|05 Supercomputing, Nov 12-18, 2005, Seattle - the International Conference on High Performance Computing, Networking, Storage and Analysis - http://sc05.supercomputing.org/

SC06, Nov. 11 - 17, 2006, Tampere Florida http://sc06.supercomputing.org/

2006 LACSI Symposium (Los Alamos Computer Science Institute):

A Sea Change in High-Performance Computing; Oct 17 - 19, 2006, Santa Fe, NM, USA http://lacsi.krellinst.org/

Other Conference Series:

The 4th Workshop on Memory Performance Issues (WMPI-2006), February 11, 2006, Austin, Texas, USA: Reconfigurable memory systems, Memory systems for vector/stream architectures, Memory-access-reducing techniques, Embedded memory systems, Fault tolerant memory systems http://www.cs.utah.edu/wmpi/2006/ in conjunction with:

HPCA-12, The 12th International Symposium on High-Performance Computer Architecture (HPCA), February 11-15, 2006, Austin, Texas, USA: Embedded and reconfigurable architectures, Interconnect and network interface architectures http://www.cse.psu.edu/conf/hpca/

HPCA-11, The 11th International Symposium on High-Performance Computer Architecture, San Francisco, Feb. 12-16, 2005: topic area explicitly listed: Embedded and reconfigurable architectures

Joint 33rd Speedup and 19th PARS Workshop[2], Basel, Switzerland, March 19 - 23, 2003. Keynote address by Prof. Reiner Hartenstein

The 20th PARS Workshop, Lübeck, Germany, June 23. - 24., 2005; topic area in Call for Papers: Interconnect Fabrics (e. g. Reconfigurable Systems)

The 10th RAW, in conjunction with IPDPS[3], Nice, France, April 2003: after a decade of non-overlap: first IPDPS people coming to attend this workshop. Keynote address: Prof. Reiner Hartenstein

The 12th Euromicro Conference on Parallel, Distributed and Network based Processing (PDP'04), La Coruña, Spain, Feb. 2004: keynote address by Prof. Reiner Hartenstein

IPDPS - International Parallel and Distributed Processing Symposium, Santa Fe, NM, USA, April 2004: keynote address by Prof. Reiner Hartenstein

HPC Asia 2004 - The 7th International Conference on High Performance Computing, July 20-22, 2004, Omiya Sonic City, Tokyo Area, Japan: Workshop on Reconfigurable Systems f. HPC (RHPC) + keynote address by Prof. Reiner Hartenstein.

HPC Asia 2005 - The 8th International Conference on High Performance Computing in Asia Pacific Region, November 30-December 3, 2005, Beijing, China, keynote by Viktor K. Prasanna, Professor, USC, Title:

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3. Preface: „Reconfigurable High-Performance Computing Systems based on conventional processors and Field Programmable Gate Arrays (FPGA) reconfigurable processors have been gaining attention. These synergistic systems have the potential of exploiting coarse-grain functional parallelism through conventional parallel processing as well as fine-grain parallelism through direct hardware execution. Many of such systems have recently been developed by major high-performance computing and reconfigurable computing vendors. For the HPCMO and DoD High-Performance Computing centers, this raises a number of questions:
   1. What is the real technology readiness level given the applications of interest?
   2. What are the sustained capabilities of such machines and how do they compare to conventional high-performance computers?
   3. Which DoD applications can benefit from hardware reconfiguration and hardware execution?
   4. What are the main considerations for a technology insertion plan?"

1.Speakers: Dr. Gordon Brebner, Distinguished Engineer, Xilinx, Kurt Dobson, Director of Engineering, Starbridge Systems, Jon Huppenthal, President and CEO, SRC, Steve Miller, Chief Engineer, SGI , Stefan Möhl, Mitrion , Dr. Walid Najjar, Professor, University of California Riverside , Dr. Viktor Prasanna, Professor, Universiy of Southern California , Virginia Ross, Rome Air Force Research Lab, Kevin L. Wohlever, Director, Ohio Supercomputer Center.

2. PARS: see http://www.iti.uni-luebeck.de/PARS/ -
3. International Parallel and Distributed Processing Symposium

Reconfigurable Computing (RC) Systems
Reconfigurable Systems (RS)
coarse grain RC platforms
algorithms
taxonomy of algorithms
software/configware co-design
configware compilers & mapping
partitioning co-compilers
reconfigurable platforms
reconfigurable gate arrays (rGAs[1])
FPGA synthesis environments
FPGA logic and circuits
FPGA physical design
FPGA circuits and technology
FPGA architectures
structured ASICs
power aware design
power aware FPGA synthesis
configware engineering
configware operating systems
basic computational models
reconfigurable computing (RC) education & curricula
RC needed in CS-related and other curricula (lobbying needed)
case studies from use in research and education
IP-based FPGA synthesis
soft CPU and array cores
reconfigurable DSP
reconfigurable instruction set processors
reconfigurable network processors

1.often also called FPGA (Field-Programmable Gate Array)

bio-computing
nano-computing
evolvable digital systems
genetic programming and algorithms
evolutionary programming and strategies
novel evolvable devices and platforms
co-evolution methods
adaptable computing systems
learning computing systems
reconfigurable supercomputing

RC went mainstream: applications found, in fact, everywhere.

reconfigurable accelerators
multi processor designs across single or multiple FPGAs
memory and I/O design
dynamically reconfigurable systems
configware scheduling and multitasking
RS design automation
compiled accelerators
Validation and verification
rapid prototyping
ASIC emulators
reconfigurable analogue and mixed-mode systems
data compression applications
RC and FPGA virus protection
security applications

reconfigurable DSP applications
reconfigurable data path arrays (rDPAs)
rDPA architectures
design space exploration
security & crypto applications
arithmetic applications
automotive and aerospace RS applications
robotics, industrial and military RS applications
multimedia and networking RS applications
other embedded systems RS applications
innovative applications
biological applications
artificial immune systems
applications in physics
applications in chemistry
applications in pharma
applications in medecine, etc.
software to configware migration
algorithms transformations
term-rewriting systems (TRS) for design and verification
testing reconfigurable systems
RS design for testability
testbeds and evolutionary design automation tools
FPGA-based fault tolerant systems
Self-repairing hardware
Self-reconfiguring hardware
placement and routing for RS
general-purpose and special-purpose design methods

Fig. 5. Subject areas for being grouped into editorial sections.

Supercomputing on Reconfigurable Platforms.

SBAC-PAD 2004 - The 16th Symposium on Computer Architecture and High Performance Computing, Foz do Iguacu, PR, Brazil, Oct 27-29, 2004: as an official topic area: Reconfigurable Systems; keynote on Reconfigurable Computing by Prof. Viktor Prasanna, USC

ISIC International Symposium on Integrated Circuits 2007 (ISIC 2007), Sept 26-28, Singapore http://www.ISIC2007.org

ISICT-2005 International Symposium on Information and Communication Technology; Capetown, South Africa, keynote address on RC (Prof. Reiner Hartenstein)

WME-2005 Workshop on Microelectronics Education, June 13, 2005, in conjunction with DAC (Design Automation Conference), Anaheim, California, keynote address on RC (Prof. Reiner Hartenstein).

CODES-ISSS 2005[1]: International Conference on Hardware/Software Codesign and System Synthesis; New York Metropolitan Area, USA, September 19-21, 2005 http://www.codes-isss.org/

Workshop on Introspective Architecture (WISA, in conjunction with HPCA-12), February 12, 2006, Austin, Texas: Self-aware, self-adaptive and self-healing architectures, Self-reconfigurable architecture http://www.cc.gatech.edu/wisa06/

ESTIMedia 2005[1]: The IEEE 2005 3rd Workshop on Embedded Systems for Real-Time Multimedia; New York Metropolitan Area, USA, September 22-23, 2005 - http://peace.snu.ac.kr/ESTIMedia/

ESTIMedia 2006: 4th Workshop on Embedded Systems for Real-Time Multimedia, Oct 26-27, Soeul, Korea

19th International Conference on Archiecture of Computing Systems, Frankfurt, Germany, March 13-16, 2006 Call for Papers includes: Reconfigurable Computing, Adaptable Computer Architecture

Annual Congress on Lateral Computing - The second International Congress on Lateral Computing, to be held by the end of 2005 at Bangalore, India, will include a special topic committee on Reconfigurable Computing. The first conference of this series had about 250 attendees.

ADCOM 2005 - The Thirteenth International Conference on Advanced Computing & Communications, December 14-17, 2005, Amrita Vishwa Vidyapeetham, Coimbatore, India, a topic area: Soft Computing; http://www.amrita.edu/adcom2005

ASICON 2005 - The 6th International Conference on ASIC, Shanghai, China, October 24 - 27, 2006, Call for Papers includes: Programmable Devices, PLD, EPLD, HDPLD, FPGA - http://www.asicon2005.com

ICESS 2005 - The 2005 International Conference on Embedded Software and Systems, December 16-18, 2005, Xi'an, P.R. China, official topic area: Reconfigurable embedded systems, http://icess05.icess.org

ISC2006 - The 21st International Supercomputer Conference, June 27 - 30, 2006, Dresden, Germany; plans to add Reconfigurable Computing to its scope, http://www.supercomp.de/

ACSAC 2006 - The 11th Asia-Pacific Computer Systems Architecture Conference, Sept. 6-8, 2006, Shanghai, PR China http://grid.sjtu.edu.cn/acsac06/index.htm

EURO-PAR 2006 - Eurpoean Conference on Parallel Computing, August 29 - September 1, 2006, Dresden, Germany http://www.europar2006.de/Download/Topics/2006_Topic18.pdf

IOLTS'06 - 12th IEEE International On-Line Testing Symposium July 10-12, 2006, Lake of Como, Italy http://tima.imag.fr/conferences/iolts/iolts06/index.html

HPCA-13 - 13th International Symposium on High-Performance Computer Architecture, Febr. 10-14, 2007, Scottsdale, Arizona, February 10-14, 2007 - http://www.hpcaconf.org/hpca13

HPCA-12 - 12th International Symposium on High-Performance Computer Architecture, February 11-15, 2006, Austin, Texas http://www.hpcaconf.org/hpca12

WISA - Workshop on IntroSpective Architectures (in conjunction with HPCA-12), February 12th 2006, Austin, Texas, USA http://www.cc.gatech.edu/wisa06/

ICS 2006 - 20th International Conference on Supercomputing, June 28 - July 1, 2006, Cairns, Australia http://www.ics-conference.org/

HiPC - HiPC 2006 International Conference on High Performance Computing, December 18 - 21, 2006, Bangalore, India http://www.hipc.org

3 Proposal of a New Journal

3.1 Proposed names of the new Journal

For the proposed new journal suitable names would be:

Reconfigurable Computing Magazine (RCM), or,
Magazine for Reconfigurable Computing (M-RC), or:
Magazine for Reconfigurable Computing and Systems (M-RCS). or
Configware Engineering Magazine (CEM)

I have heard (and I will investigate this for details), that a private publisher has introduced a journal with the name of ***Reconfigurable Computing***.

1. The call for papers lists: reconfigurable platforms (under ... Architecture), reconfigurable processors (under: Application-specific Architectures and Synthesis)
1. organized under IEEE/ACM/IFIP CODES+ISSS 2005 Conference - the call for papers lists: multimedia processors and reconfigurable architectureds

3.2 Members of the Board of Editors

For the first year, or, for the first two years I would like to be a candidate for EIC. For membership of the editor search committee I would like to propose (in alphabetical order): Prof. Dr. Neil Bergman, University of Queensland, Brisbane, Australia; Prof. Dr. Toshiaki Miyazaki, University of Osaka, Japan, Prof. Dr. Viktor Prasanna, USC. Also by myself, I would like to be a candidate for joining the search committee.

Reiner Hartenstein	
google	yahoo
12,100	8,930

Fig. 6. Google found ... (October 2005)

3.3 Proposed editorial policy

The new journal should use the same layout style as given by the flagship magazine to obtain a brother and sister look stressing the dual-paradigm approach to make computing sciences more fascinating to young people, as well as, to win well established professionals to join the dual mind set for teaching by upgraded common models.

The following regular columns should be discussed to meet the desirable missions of the new journal:

Reconfigurable Systems. Reconfigurable Computing Systems, adaptable computing systems, FPGA-based and FPGA-like computing engines, compiled accelerators, coarse grain RC platforms, architectures, compilation methods, system-on-chip (SoC) applications, educational deficits, lobbying for curricular updates

The wrong roadmap. High Performance Computing (HPC), supercomputing, the missed role of reconfigurable accelerators, educational deficits, tutorials, surveys, critical status reports, proposing new directions in R&D, lobbying for curricular updates

reconfigurable Gate Arrays (rGAs, or, FPGAs). synthesis environments, FPGA logic and circuits, circuits and technology, novel FPGA circuits and circuit-level techniques, synthesizable embedded programmable logic cores, physical design, architectures, pipelined FPGAs for embedded processors, applications, FPGA-based and FPGA-like computing engines, compiled accelerators, structured ASICs, power aware design with FPGAs, power aware FPGA architecture synthesis, novel logic block and routing architectures, combination of FPGA fabric and system blocks (processors, etc.), new commercial architectures, impact of modern and future technologies (including ultra-deep submicron and nanometer scale) on the design of FPGAs (e.g. soft errors, leakage, power density, fabrication defects), nano technology FPGAs

Applications. case studies, innovative use of FPGAs, exploitation of FPGA features, novel circuits, high-performance and low-power/mission-critical applications, DSP techniques, uses of reconfiguration, FPGA-based cores, commercial applications, speed-up factors, speed-up mechanisms, algorithms, architectures, security applications, reconfigurable DSP applications, reconfigurable data path arrays (rDPAs), rDPA architectures, design space exploration, security & crypto applications, arithmetic applications, automotive and aerospace RS applications, robotics, industrial and military RS applications, multimedia and networking RS, other embedded systems RS applications, innovative applications, biological applications, artificial immune systems, and many more application areas.

Configware. compilation methods, configware/software co-compilation, operating systems for dynamically reconfigurable platforms, configware scheduling and multitasking, configware design flows, configware design automation, IP-based configware implementation, configware engineering education.

Configware Operating Systems is an area of its own, since being fundamentally different from classical software operating systems, covering: dynamically reconfigurable systems, configware scheduling and multitasking.

Algorithms. taxonomy of algorithms, taxonomy of application areas in reconfigurable computing, taxonomy of interconnect requirements for software-to-configware migration, algorithms transformations, term-rewriting systems (TRS) for design and verification.

Bio-informatics and biology-inspired reconfigurable computing. bio-computing, nano-computing, reconfigurable DNA processing systems, evolvable digital systems, genetic programming and algorithms, evolutionary programming and strategies, novel evolvable devices and platforms, co-evolution methods, artificial evolution, evolutionary methods for design, optimization and control, evolutionary robotics.

Reconfigurable high performance Computing Systems. adaptable computing systems, learning computing systems, reconfigurable supercomputing, coarse grain reconfigurable accelerators, multi processor designs across single or multiple FPGAs, memory and I/O design.

Rapid prototyping. FPGA (rGA) and rDPA use for rapid prototyping, ASIC emulators, logic emulation,

reconfigurable analogue and mixed-mode systems, design flows, fast prototyping for system-level design, Multi-Chip Modules (MCMs).

Security applications. RC and FPGA damaging viruses, virus protection using FPGAs, security applications, crypto applications, artificial immune systems.

Coarse grain reconfigurable systems. reconfigurable data path arrays (rDPAs), rDPA architectures, design space exploration, compiled accelerators, reconfigurable computing, adaptive computing devices, systems and software, arithmetic applications, supercomputing, reconfigurable DSP applications, biological applications.

Embedded system applications. automotive and aerospace RS applications, robotics, industrial and military RS applications, data compression applications, communication, wireless communication applications, multimedia and networking RS applications, consumer electronics applications, facility management support applications, sensor networks, many other embedded systems RS applications.

Design automation and testing. compiled accelerators, software/configware co-compilers, automatic software/configware partitioning, software/configware/hardware partitioning, validation and verification, term-rewriting systems (TRS) for design and verification, testing reconfigurable systems, RS design for testability, testbeds and evolutionary design automation tools, CAD for FPGAs, Placement, routing, logic optimization, technology mapping, system-level partitioning, logic generators, testing and verification, CAD for FPGA-based accelerators, CAD for incremental FPGA design.

FPGA-based fault tolerant systems. Self-repairing hardware, dynamically reconfigurable platforms, self-reconfiguring hardware, incremental placement and routing for RS, configware scheduling and multitasking, general-purpose and special-design methods.

For many areas of reconfigurable computing good surveys, taxonomies, and good tutorials are missing. The following columns cannot be offered regularly, since it is difficult to solicit such submissions:

Surveys. rDPAs, FPGAs, architectures, applications, configware industry, configware engineering, RS design automation, basic paradigms, business models.

Taxonomies. rDPAs, FPGAs, architectures, applications, algorithms.

Tutorials. rDPAs, FPGAs, architectures, applications, configware engineering, RS design automation, basic paradigms, business models.

3.4 The promising market of the proposed new journal

RC meanwhile is penetrating practically all application areas of computing sciences and microelectronics design (see Fig. 5.), which creates an enormous demand by researchers and developers publishing their results. But because of the fundamentally different mind set resulting in the configware / software chasm existing magazines like e. g. CACM or IEEE Computer are no suitable publication platforms for the wide variety of RC and related areas, but should provide sufficient space to cover the essentials of common interest on Reconfigurable Computing and all its application areas[1].

An important means to get publicity is it, to discuss the RC-related curricular backlag problems. I am ready to cooperate with curricular committees and to get other persons from RC involved here. Existing journals also are not ready to attack problems in lobbying curricular updating to cope with the configware / software chasm. and, for heading toward the final break-through by spreading RC-related innovative ideas in academia, industry and government. All the challenges coming with such efforts cannot be met without using a new journal dedicated to meet such goals. As soon as the RC-related educational deficits of the traditional computing scenes have been substantially reduced, which might take at least a decade from now, a merger between the current flagship magazine and the proposed new journal may be discussed.

For me it is not a problem[2] to propose a major number qualified experts from the US, and, from all over the world, being ready to help as members of the editorial board of the proposed journal and for writing editorials and special columns, as well as for soliciting submissions from a wide variety of RC core scenes and application communities. It is no problem to set up a structure of regular editorial sections, not only from the items shown by Fig. 5. I am ready to set-up a more detailed proposal within a few weeks.

1. R. Hartenstein: What means Reconfigurable Computing ? (Computer Societies should catch up); http://hartenstein.de/RC/WhatMeansRC.html

2.Reiner Hartenstein is and has been member of numerous program committees and three steering committees in the field and have been four times a program chair of FPL and two times of RAW. Frequently being invited to give RC-related invited talks or keynote addresses at international conferences I am well familiar with the hot spots and trends in the field

4 CV of Reiner Hartenstein

Reiner Hartenstein received all his academic degrees from the EE department of the Universitaet Karlsruhe (TH). Reiner Hartenstein is professor (emeritus) of CS (Informatik) at Kaiserslautern University of Technology (TU Kaiserslautern), Germany. He is expert on Reconfigurable Computing, VLSI design automation and computer architecture. He received all academic degrees from the EE department of the Universitaet Karlsruhe (TH), Germany. His mentor (advisor of his Master thesis and Ph. D. thesis) has been Karl Steinbuch[1], pioneer in artificial neuronal networks and co-founder of German academic CS programs. See: http://helios.informatik.uni-kl.de/euology.pdf

IEEE life fellow, FPL fellow, best paper awards, 50 invited talks, mostly keynotes, since year 2000, founder of 4 conference series, founder of E.I.S. German multi-university VLSI design project[1].

1. following the Mead-&-Conway movement

Reiner Hartenstein is founder of the PATMOS[2] series of annual international low power VLSI design conferences[3], as well as of the Mead-&-Conway-style German Multi-University VLSI design „E.I.S“. Project[4], a forerunner of the Eurochip organization supported by the commission of the European Union. He is co-founder of the FPL[5] annual international conference series and of EUROMICRO[6], running several international conference series. He is co-founder of EUROMICRO's first conference within this program of several international conferences: the EUROMICRO symposium series on the microarchitecture of computer systems, which he has opened up in 1975 at Nice, France.

Reiner Hartenstein is and has been a member of numerous international steering committees and program committees and has been general chair and ten times program chair of international conferences - four times of an FPL conference (see above) and two times of the RAW workshop (see above).

Reiner Hartenstein has published 415 professional papers and has authored, edited, or co-edited 14 books.

Reiner Hartenstein and his team have received several best paper and best presentation awards. Hartenstein has been honored by the titles of IEEE fellow and FPL fellow. More recently Reiner Hartenstein is frequently invited to international conferences, also to HPC and supercomputing conferences, for giving invited presentations or keynote addresses on Reconfigurable Computing. In 2004 Reiner Hartenstein has also been invited to open by his keynote address a newly founded workshop on Reconfigurable Systems for High Performance Computing (RHPC) running in conjunction with the Asia HPC Conference (this time at Omiya, Japan, June 2004).

New workshop series to be started in 2006. Reiner Hartenstein is the founder and general chair of a new international workshop series on *Reconfigurable Computing education* (RC education[7]), beginning at Karlsruhe, Germany, March 1, 2006, in conjunction with the **IEEE Computer Society** Annual Symposium on VLSI, March 2–3, 2005, Karlsruhe, Germany. Reiner Hartenstein plans, to have the 2nd workshop of this series in 2007 run by the **IEEE Computer Society**. For around mid of 2006 Reiner Hartenstein plans to propose a special issue of the COMPUTER magazine on Reconfigurable Computing, also to publish selected papers from the 1st RC education workshop.

1. Bernard Widrow (Stanford University), Reiner Hartenstein (TU Kaiserslautern), Robert Hecht-Nielsen (University of California, San Diego): „1917 Karl Steinbuch 2005“; IEEE Computational Intelligence Society Newsletter, August 2005, downloadable from: http://helios.informatik.uni-kl.de/euology.pdf
2. http://www.fpl.uni-kl.de/conferences/patmos/patmos.html --- http://www.patmos-conf.org/
3. world-wide the oldest conference series on low power microelectronics design, still growing
4. Lynn Conway called him „the German Carver Mead“ -- http://xputers.informatik.uni-kl.de/staff/hartenstein/eishistory_en.html
5. the International Conference on Field-Programmable Logic, Reconfigurable Computing and Applications - world-wide the oldest and largest conference in the field ---- http://fpl.org
6. http://www.euromicro.org/
7. http://helios.informatik.uni-kl.de/RCeducation/

5 Reconfigurable Computing Glossary

accelerator. hardware or morphware connected to a von Neumann (vN) architecture for algorithms running too slow on vN. Example: graphics board or chip in a PC. Most accelerators' machine paradigm is data-stream-based.

Anti machine. data-stream-based machine (fig.3 b), the counterpart to the von Neumann machine: uses one or several *data counters* instead of a program counter. It has no vonNeumann bottleneck. The anti machine is parallel by its nature: it can run several data streams in parallel - like a combustion engine having multiple cylinders.

ASM (auto-sequencing memory). includes a data counter (fig.3 b, compare „anti machine")

ASMA (ASM array). distributed memory of a parallel anti machine (fig.3 b)

Morphware. structurally programmable hardware (introduced by DARPA-funded projects to stress the contrast to „hardwired" and to avoid the fuzzy term „soft hardware").

CLB. Configurable Logic Block: about a single bit wide programmable logic resource

Configware. structural programming source or code for morphware: its basic paradigm is different from that of software. Configware compilers have to generate two different kinds of code: structural code and data scheduling code (see fig 2 c/d)

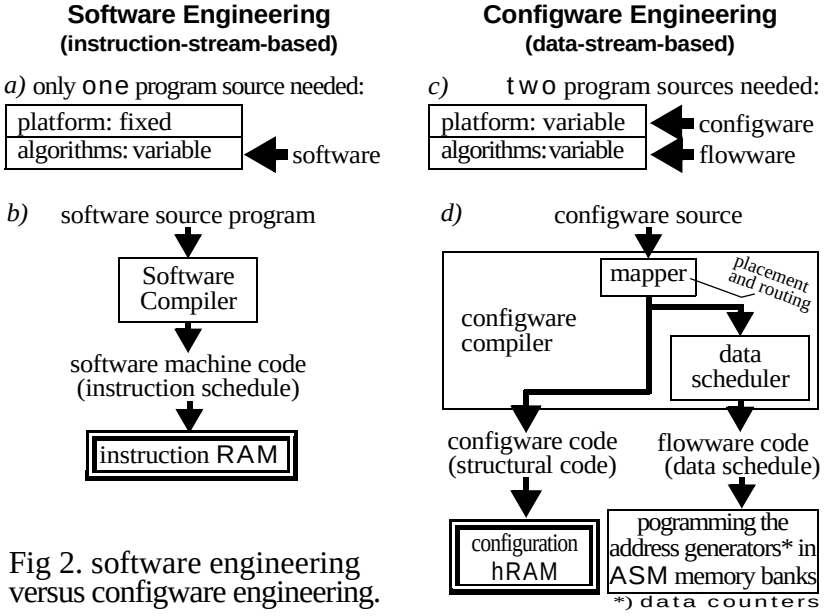

Fig 2. software engineering versus configware engineering.

coarse-grained Morphware. Since rDPAs (reconfigurable Data Path Arrays) have wide data path width, as for example, 32 bits, those are called „**coarse-grained** reconfigurable" - much more area-efficient than FPGA and microprocessor: more than a hundred DPUs fit onto a single microchip.

CPU. execution unit of the von Neumann machine - includes a *program counter* (fig 3 a)

data counter. see „anti machine" (also see fig 3 b)

data stream. by context of Reconfigurable Computing this term follows the definition created for the systolic arrays about 25 years ago

DPA (data path array). array of DPUs (fig.3 b), a generalization of the systolic array such, that reconfigurability makes sense (see rDPA).

DPU (data path unit). execution unit of the anti machine - **does not include** a program counter (fig.3 b). Execution is data-transport-triggered.

dual paradigm. to-day, the de facto common model of computing is the symbiosys of both paradigms: von Neumann and anti machine

fine-grained Morphware. Since a CLB is only about a single bit wide, FPGA are called „**fine-grained** reconfigurable".

Flowware. program source or code to generate data streams (fig 2 b).

FPGA. Field-Programmable Gate Array, fine-grained morphware platform

GAG (generic address generator). data sequencer used inside ASM to manipulate the data counter (fig 3 b) - a generalization of the DMA.

hidden RAM (hRAM). a distributed background memory inside a morphware platform accepting downloaded ***Configware*** code: s. fig 2 b). This downloading is comparable to booting as known from classical computers.

hRAM. see „hidden RAM"

rDPA. reconfigurable *DPA*, reconfigurable to form a pipe network (fig.3 b)

rDPU. reconfigurable *DPU* (fig.3 b), e. g. component of a rDPA

Software. instruction-stream-based programming source or code for classical computers - this term should **not** be used for morphware programming sources or code (also see fig 2)

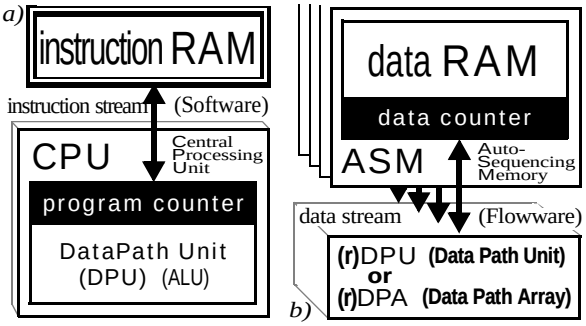

Fig 3. basic paradigms: a) von Neumann machine, b) anti machine (reconfigurable or fixed).

von Neumann machine (vN). instruction-stream-based machine - counterpart to the *anti machine*: uses a single program counter instead of data counters. In contrast to the anti machine, the vN machine is sequential by its nature: it can handle only a single instruction stream.

platform		program source or code	machine paradigm
Hardware (hardwired logic)		(no program)	(none)
Morphware	reconfigurable logic	***Configware***	
	Reconfigurable Computing	***Configware + Flowware***	anti machine (AM)
hardwired processor	data-stream-based [e.g. Broderson]	***Flowware***	
	instruction-stream-based	***Software***	von Neumann (vN)
embedded systems + reconfigurable supercomputing, etc.		***Software + Configware + Flowware***	dual paradigm: vN + AM

Fig 4. contemporary double-paradigm terminology (compare fig. 2).