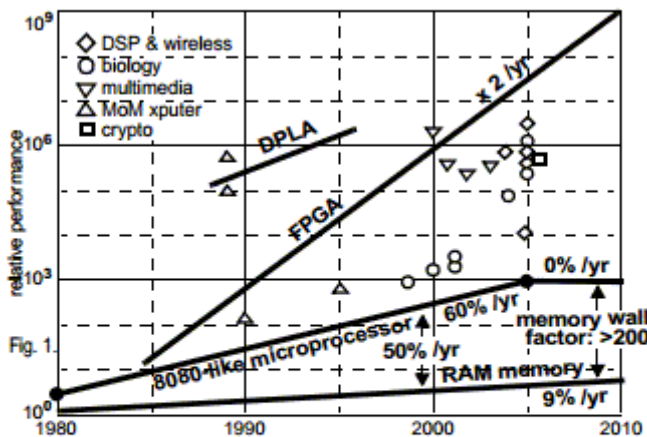


Speed-up Factors

Reiner Hartenstein, IEEE fellow, FPL fellow, SDPS fellow <http://hartenstein.de>, April 2012

Selection from a paper (2006) by Reiner Hartenstein, TU Kaiserslautern



Compared to software implementations sensational speed-up factors have been reported for software to configure migrations by using FPGAs. Fig. 1 shows a few speedup factors picked up from literature, reporting a factor of 7.6 in accelerating radiosity calculations [1], a factor of 10 for FFT (fast Fourier transform), a speedup factor of 35 in traffic simulations [2]. For a commercially available Lanman/NTLM Key Recovery Server [3] a speedup of 50 - 70 is reported. Another cryptology application reports a factor of 1305 [5]. A speedup by a factor of 304 is reported for a R/T spectrum analyzer [7]. In the DSP area [8] for MAC [8] operations a speedup factor of 100 has been reported compared to the fastest DSP on the market (2004) [9]. Already in 1997 versus the fastest DSP a speedup between 7 and 46 has been obtained [10]. In

Biology and genetics (also see [11] [11]) a speedup of up to 30 has been shown in protein identification [13], by 133 [14] and up to 500 [15] in genome analysis, as well as 288 with the Smith-Waterman pattern matching algorithm at the National Cancer Institute [17]. In the multimedia area we find factors ranging from 60 to 90 in video rate stereo vision [18] and from 60 to 90 in real-time face detection [19], and of 457 for hyperspectral image compression [20]. In communication technology we find a speedup by 750 for UAV radar electronics [21]. These are just a few examples from a wide range of publications [23] [24] [26] [27] [28] [30] [32] reporting substantial speedups by FPGAs.

For an updated version picture [33] see: <http://www.fpl.uni-kl.de/staff/hartenstein/Fig-15-speed-up.pdf>

Literature:

- [1] A. A. Gaffar and W. Luk: Accelerating Radiosity Calculations; FCCM 2002
- [2] M. Gokhale et al.: Acceleration of Traffic Simulation on Reconfigurable Hardware; 2004 MAPLD International Conference, Sept. 8-10, 2004, Washington, D.C., USA
- [3] F. Dittrich: World's Fastest Lanman/NTLM Key Recovery Server Shipped; Picocomputing, 2006 URL: [4]
- [4] <http://www.picocomputing.com/press/KeyRecoveryServer.pdf>
- [5] K. Gaj, T. El-Ghazawi: Cryptographic Applications; RSSI Reconfigurable Systems Summer Institute, July 11-13, 2005, Urbana-Champaign, IL, USA URL: [6]
- [6] <http://www.ncsa.uiuc.edu/Conferences/RSSI/presentations.html>
- [7] J. Hammes, D. Poznanovic: Application Development on the SRC Computers, Inc. Systems; RSSI Reconfigurable Systems Summer Institute, July 11-13, 2005, Urbana-Champaign, IL, USA
- [8] *ASM* = Auto-Sequencing Memory; *DSP* = Digital Signal Processing; *EDA* = Electronics Design Automation; *ESL* = Electronic System-Level Design; *FIR* = Finite Impulse Response; *FPGA* = Field-Programmable Gate-Array; *MAC* = Multiply and Accumulate; *PU* = Processing Unit *rDPA* = reconfigurable Data Path Array; *rDPU* = reconfigurable Data Path Unit; *rE* = reconfigurable Element
- [9] W. Roelandts (Keynote-Adress): FPGAs and the Era of Field Programmability; International Conference on Field Programmable Logic and Applications (FPL), Aug. 29 - Sept 1, 2004, Antwerp, Belgium,
- [10] J. Rabaey: Reconfigurable Processing: The Solution to Low-Power Programmable DSP, Proc. ICASSP 1997
- [11] Y. Gu, et al.: FPGA Acceleration of Molecular Dynamics Computations; FCCM 2004 URL: [12]
- [12] <http://www.bu.edu/caadlab/FCCM05.pdf>
- [13] A. Alex, J. Rose et al.: Hardware Accelerated Novel Protein Identification; FPL 2004
- [14] N. N. Nallatech, press release, 2005
- [15] H. Singpiel, C. Jacobi: Exploring the benefits of FPGA-processor technology for genome analysis at Acconovis; ISC 2003, June 2003, Heidelberg, Germany URL: [16]
- [16] <http://www.hoise.com/vmw/03/articles/vmw/LV-PL-06-03-9.html>
- [17] N. N. (Starbridge): Smith-Waterman pattern matching; National Cancer Institute, 2004
- [18] A. Darabiha: Video-Rate Stereo Vision on Reconfigurable Hardware; Master Thesis, Univ. of Toronto, 2003
- [19] R. McCready: Real-Time Face Detection on a Configurable hardware Platform; Master thesis, U. Toronto
- [20] T. Fry, S. Hauck: Hyperspectral Image Compression on Reconfigurable Platforms; IFCCM 2002
- [21] sP. Buxa, D. Caliga: Reconfigurable Processing Design Suits UAV Radar Apps; COTS Journal, Oct. 2005 URL: [22]
- [22] http://www.srccomp.com/ReconfigurableProcessing_UAVs_COTS-Journal_Oct05.pdf
- [23] <http://helios.informatik.uni-kl.de/RCeducation/>
- [24] R. Porter: Evolution on FPGAs for Feature Extraction; Ph.D. thesis; Queensland Un. of Technology Brisbane, Australia, 2001 : [25]
- [25] http://www.pooka.lanl.gov/content/pooka/green/Publications_files/imageFPGA.pdf
- [26] E. Chitalwala: Starbridge Solutions to Supercomputing Problems; RSSI Reconfigurable Systems Summer Institute, July 11-13, 2005, Urbana-Champaign, IL, USA
- [27] S. D. Haynes, P. Y. K. Cheung, W. Luk, J. Stone: SONIC - A Plug-In Architecture for Video Processing; FPL 99
- [28] M. Kuulusa: DSP Processor Based Wireless System Design; Tampere Univ. of Technology, Publ. No. 296; URL: [29]
- [29] <http://edu.cs.tut.fi/kuulusa296.pdf>
- [30] B. C. Schäfer, S. F. Quigley, A. H. C. Chan: Implementation Of The Discrete Element Method Using Reconfigurable Computing (FPGAs); 15th ASCE Engineering Mechanics Conf., June 2-5, 2002, New York, NY, URL: [31]
- [31] <http://www.civil.columbia.edu/em2002/proceedings/papers/126.pdf>
- [32] G. Lienhart: Beschleunigung Hydrodynamischer N-Körper-Simulationen mit Rekonfigurierbaren Rechen-systemen; Joint 33rd Speedup and 19th PARS Workshop; Basel, Switzerland, March 19 - 21, 2003
- [33] Tarek El-Ghazawi, Esam El-Araby, Miaoqing Huang, Kris Gaj, Volodymyr Kindratenko, and Duncan Buell, "The Promise of High-Performance Reconfigurable Computing," IEEE Computer, vol. 41, no. 2, pp. 69-76, February 2008