CVT Software Catalogue; Annex A1, CVT final report, May 1986

Task 1: Architecture

1.1	AVST	Automated verification system of temporal properties
1.2	ABLED	Register-transfer level schematic editor
	ABLTOKARL	ABL to KARL translator
1.3	CML	C microprogramming language and compiler
1.4	PNP	Editor and simulator for protocol models
1.5	CFS/PLA	PLA-base finite state machines generator
1.7	KARL III	Register-transfer level language, compile: and simulator
1.8	ALGIC	General silicon-compiler system
	ALGIC-DSP	DSP silicon compiler
	MODGEN	nMOS module generator
	ROMGEN	CMOS module generator
1.9	GASCON	Control parts generator
1.10	DACAPO-II	Multi-level simulation system
	CAPSYN-C	Self-timed controller synthesis tool
1.11	TESEV	Test set evaluator
	RECOM	Simulation result comparison tool

Task 2: CVT system framework; tools for layout design and verification

2.1	COSMIC	CVT data base manager
2.2	MONITOR	User interface and supervisor of CVT system
	EDICVT	Layout editor
2.3	MDMOS	Set of tools for logic-gates based design
2.4	SYMBAD	Leaf block symbolic design
2.6	PLEX	Parameter and logical extractor
	TIMCALC	Delay calculation for timing analysis
2.7	SELLAV	Procedural layout tool
2.8	ALT	Layout transformation tool
2.9	DNX	DECnet emulation package
	BRUTUS	Hierarchycal design rule checker
	PUTCIF-EXTRCIF	CIF-COSMIC converter
2.10	DOMOS	Transient circuit simulator
	DOSCA	Switched-capacitor simulator
	DIGIT	Signal flow-graph level simulator

Task 3: Testing

3.2	BAT	Behavioural automatic tester
	FERT	Fault-model generator at RT-level
	TIGER	Test-pattern generator at RT-level
3.4	OFGKA	Fault generator at RT-level
	OFSKA	Fault simulator at RT-level
	OTAKA	Testability analysis program at RT-level
3.5	DTSV	Simulator and test generator at logic level

Task 4: Device modeling

4.3	DAMSEL	Data manager
	SODA	Compiler
	IDAS	Interactive device analysis environment
	ATMOS	Mesh generator
	DAMIGO	Graphic package
	TRMESH	Mesh generator
	M2D	Mesh generator
	VIS3D	3D visualization
	CAPA	Parasitic capacitance evaluator
	PROPIV	Linear solver
	MSHPTS	Mesh generator
	SIOUDA	Simulation of indexed organization
4.4	HFIELDS	Device simulator
	JUPIN	Device simulator
4.7	TAB	Table-model generator