Abstract (Preface)

We need more Computing Services
But the Energy Consumption of Computing worldwide will become unaffordable.
And the Performance Progress is stalled by the Parallelism Wall and the Power Wall
Reconfigurable Computing (RC) could be a Silver Bullet to solve such Problems
However all this is massively handicapped by Programmer Productivity Problems etc.
We need to reinvent Computing.
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Outline
• The coming Shortage of Energy
• Why Computing is important
• Energy Consumption of Computing
• The Programmability Crisis
• Rescue by Reconfigurable Computing?
• The Reconfigurability Paradox
• We need to Reinvent Computing
• Reinventing Programmer Education
• Conclusions
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The Twin Wall Crisis: Power & Performance
Worldwide two drastically disruptive Developments:
µP Industry changed Strategy over to „manycore“ (away from faster Clock Speed)
The Programming Wall
A Variety of Power Consumption Problems
The Power Wall
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No more cheap oil
Currently: >80 $
Tendency: growing
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Oil crises: weekend driving ban (Germany)
(depenence on near east oil countries)
1973
1979/1980
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Keynote, The 1st Brazilian-German Workshop on Micro and Nano Electronics (BGME’2010), October 6 - 8, 2010, Porto Allegre, RS, Brazil
Beyond Peak Oil

Cheap Oil Era reached its End

Beyond Oil: Literature

Outline

Banking without Computers
Computing is important
Survival and Success of the global Economy
We have to convince all Funding Sources

Business Information Systems without Computers
Lufthansa Reservation anno 1960
http://wiki.answers.com/Q/Why_are_computers_important_in_the_world

Computers everywhere

... Ecosystem: just one example

... Supercomputers ...

Data Centers ...
Self Near Leisure conflict avoidance

Reduce testing and integration time and costs of complex CPS systems

Physical critical infrastructure that calls for preventive maintenance,

Rescue by Reconfigurable Computing?

Support of the Elderly

The Reconfigurability Paradox

Safe, rapid evacuation in response to natural or man-made disasters

Carpooling and public transport by info web sites

Assistive Devices

promotion of shared values

Conclusions

Energy Consumption of computing

Environment

Communication

We need to Reinvent computing

human security

Computing will play a key part in global risk management

The amount of infrastructure making up the digital world is increasing

Intelligent water management

We are experiencing a shift to the digital world in our daily lives

Smart energy meters: housing, buildings, facilities

Mobility

economic growth

Simulation and modelling are important tools which will help predict global warming and its effects

Health

Sustainable development

The coming shortage of energy

poverty eradication

Energy

global vaccine protocol

Reinventing programmer education

Location

climate protection

The programmability crisis

Road traffic and transport logistics optimization

Quality of life

Disaster response: large scale emergency evacuation

Extreme

penning de fries: list by Rene

• Security

• Mobility

• Communication

• Health

• Bio-medical

• Support of the elderly

• Quality of life

• Leisure

• Environment

• Sustainable development

• Energy

Trends (Glesner’s list):

List by Rene Penning de Fries:

• Energy

• Water

• Food

• Environment

• Poverty

• Terrorism

• War

• Disease

• Education

• Democracy

• Population (2050: ~10 billion people)

Growing number of computers

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• Energy consumption of computing

• The programmability crisis

• Rescue by reconfigurable computing?

• The reconfigurability paradox

• We need to reinvent computing

• Reinventing programmer education

• Conclusions

Some grand challenge examples for CPS [Ed. Lee]

• Blackout-free electricity generation and distribution

• Extreme yield agriculture

• Safe, rapid evacuation in response to natural or man-made disasters

• Perpetual life assistance for busy, senior/disabled people

• Location-independent access to world-class medicine

• Near-zero automotive traffic fatalities, minimal injuries, and significantly reduced traffic congestion and delays

• Reduce testing and integration time and costs of complex CPS systems (e.g. aircraft) by 1 to 2 orders of magnitude

• Energy-aware buildings and cities

• Physical critical infrastructure that calls for preventive maintenance

• Self-correcting cyber-physical systems for “one-off” applications

• Disaster response: large scale emergency evacuation

• Assistive devices

Innovation-driven computing

• Simulation and modelling are important tools which will help predict global warming and its effects

• The amount of infrastructure making up the digital world is increasing to grow rapidly and starting to consume significant energy resources

• Computing will play a key part in optimizing use of resources in the physical world

• We are experiencing a shift to the digital world in our daily lives as witnessed by the wide scale adoption of the world wide web

• To help generate momentum and achieve these goals, it is important that a coordinated set of challenging international projects are investigated

Green IT:

• Smart energy meters: housing, buildings, facilities

• Carpooling and public transport by info web sites

• Road traffic and transport logistics optimization

• Reduce travelling by telecommuting

The world economic forum’s “global redesign initiative”

“Existing global institutions require extensive reworking to confront contemporary challenges.”

Organizations like UN, UNESCO; GATT, G8, G20 are increasingly inept at fixing what ails the world:

• economic growth

• climate protection

• poverty eradication

• conflict avoidance

• human security

• global vaccine protocol

• global risk management

• promotion of shared values

• intelligent water management

• smart energy production/distribution

Wikinomics approach: for agile world-wide mass collaboration without bureaucracy

New paradigm to involve world citizens by global IT networks with graphic user interfaces for citizen juries, polling, digital brainstorming, policy meetings...

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Growth of the Internet

The trends are illustrated by:
- expanding wireless internet
- growing number of users
- shipping electronic books
- more cloud computing?
- and many other services.

2007 to 2030 factor x30 predicted

[Google claims 2% of the world's electricity consumption now]

Power Consumption of Computers

Exascale (10^18) supercomputer predicted for ~2020: 120 MW

“Largest supercomputers, including exoflaps, should not be thought of as computers. They're strategic scientific instruments. Their usage patterns and scientific impact are closer to major facilities such as CERN, ITER, or Hubble.”

[Andrew Jones, Numerical Algorithms Group, 2008]

Energy cost may overtake IT equipment cost in the near future

“Google causes 2% of the world’s electricity consumption”

[Google denied]

How Societies Chose to Fail or Succeed

Manycore: failure could jeopardize both IT industry & most sections of the economy depending on rapid improvement of IT.

[Dave Patterson]

Several recent outages of cloud computing services.

Unaffordability of von-Neumann-centric computing could jeopardize all facets of our global economy.

Stuxnet worm: only propaganda trick?

How Societies Chose to Fail or Succeed

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[Dave Patterson]

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Stuxnet worm: only propaganda trick?

Electricity Bill: a Key Issue

Patent for water-based data centers

- Already 2005, Google's electricity bill higher than value of its equipment.

Google data center cost determined by monthly power bill

“... the possibility of computer equipment power consumption spiraling out of control could have serious consequences for the overall affordability of computing.”

[L. A. Barroso, Google, 2009]

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The Trouble with Manycore

The growing core counts are racing ahead of programming paradigms and programmer productivity.

Chipmakers busy designing microprocessors that most programmers can’t program...

[David Patterson, IEEE Spectrum, July 2010]

... doing so without any clear notion of how such devices would in general be programmed.

They hope, someone will be able to figure out how to do that.

going to FPGA: for programmers a paradigm shift - a challenge to CS education.

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Multicore is not new

Dead (Super)Computer Society

- AGRI
- Alliant
- American Supercomputer
- Amos
- Advanced
- Applied Dynamics
- Astronautics
- BBN
- CDC
- Convex
- Cygnus
- Cycore
- Cycore Research
- Custer-Harris
- Custer Scientific
- Cydrome
- Dana/Ardent
- Stellar/Stardent

the single core sequential mind set was the winner

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Can we get it right this time?

The “parallel programming problem” has been addressed for at least 25 years.

Only a small number of specialized developers can write parallel code.

A massive worldwide effort is required, taking many years, creating masses of jobs.

“Foundational change will disrupt traditional habits throughout the discipline”...

[Michael Wrinn, keynote, SIGCSE2010]

We need to reinvent computing

We need to reinvent programmer education

“...The proud era of von Neumann architecture passes into history.”

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 Amid the Clamor

current discussions: despairingly seeking a needle in a haystack.

How to bring parallel computing into mainstream of undergraduate education?

[Micahel Wrinn]

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We need a new Textbook

Manycore Programming for Dummies

A Reference Guide For The Perplexed

having an impact like Mead & Conway

“The book that changed everything”;

Electronic Design News, Feb. 11, 2009

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Twin paradigm systems
design start ratio ASIC: 3%
FPGA: 97%
[Dataquest, 2009]
However, it needs accelerators
Central: it controls (almost) everything
CPU accelerators
second paradigm
CPU accelerators
hardwired accelerators
reconfigurable accelerators

A Clean Terminology, please
program source instruction streams
Flowware data streams
Configware datapath structures configured

Power savings factors obtained (FPGAs)
Energy saving factors: ~10% of speedup

…
FPGA vs. x86 Clock Frequency

Celeron to Pentium IV: x20
growing clock speed
growing power consumption
(migration papers: power save not reported before 2005)

-> not obsolete!!

Hitting 28nm, and beyond

Both de-facto FPGA giants (Xilinx and Altera) are hitting 28nm at end of 2010.

2009: Intel ships 32nm,
2010: foundries to ship 28nm
Intel will ship 22 nm in 2011,
16 nm in 2013

Also FPGAs benefit from Technology progress.
New Xilinx and Altera products push the power limits
also for FPGA use in battery-powered small portables
(IGLOO from Altera, from Xilinx: 28 nm low-
power process at TSMC and Samsung Foundry)

RC*: Demonstrating the intensive Impact

Application | Speed-up factor | Power | Cost | Size
--- | --- | --- | --- | ---
DNA and Protein sequencing | 8723 | 779 | 22 | 253
DES breaking | 28514 | 3439 | 96 | 1116

Hetero HPC

SGI® RASC™

SGI® RASC™ Module (Variant)
Xilinx Virtex II 8000 FPGA
16MB QDR SRAM
Rack-mountable
Dual NUMAlink™ 4 ports
Seamless direct attach to server’s shared memory fabric
Datasheet (PDF 145K)

SGI® RASC™ RC100 Blade
Dual Virtex 4 L200 FPGA
80MB QDR SRAM or 256G DDR2 2GDRAM
Blade in main-processor form factor
Dual NUMAlink™ 4 ports
Seamless direct attach to server’s shared memory fabric
Datasheet (PDF 137K)

The silver bullet

Scene | Green Computing | Reinvent Computing
--- | --- | ---
predicted energy saving | factor of about 3 | orders of magnitude
Reconfigurable Computing is really the silver bullet for massively saving energy

For instance: a hangar full of racks replaced by a single rack
without air conditioning or ½ rack

END
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FPGA: much worse Technology?

- Lower Clock Frequency (x3 – x5)
- huge Wiring Overhead (for routing)
- Reconfigurability Overhead: e. g. only about 4 % of Transistors serve the Application & Routing Congestion ...
- Speed-up by Orders of Magnitude with an Orders of Magnitude worse Technology?
- The Reconfigurability Paradox

The von Neumann Syndrome

More power for creating foam than to accelerate the vessel?

the tremendous inefficiency of computers causes immense electricity consumption

Massive Overhead Phenomena

overhead

von Neumann
machine

instruction fetch

state address computation

data address computation

data meet PU + other overhead.

transactional memory overhead

message passing overhead

inter PU communication

overproportional to the number of processors

overproportional to the number of processors

Critique of the von Neumann Model

Nathan's Law: Software is a gas. It expands to fill all its containers ... Nathan Myhrvold

Wirth's Law
software is slowing faster than hardware is accelerating

Peter G. Neumann 1985-2003: 216x

overhead piles up to code sizes of astronomical dimensions

Critique of von Neumann is not new:

Dijkstra 1968: The Goto considered harmful

R. Hartenstein, G. Koch 1975: The universal Bus considered harmful

Backus 1978: Can programming be liberated from the von Neumann style

Arvind et al., 1983: A critique of Multiprocessing the von Neumann Style

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**Featuritis & Overhead**

Software is too easy to change: Overhead, Featuritis, and: Bugs

Configware is less easy to change: a highly important advantage?

---

**von Neumann overhead vs. Reconfigurable Computing**

<table>
<thead>
<tr>
<th>overhead</th>
<th>von Neumann machine</th>
<th>datastream machine</th>
</tr>
</thead>
<tbody>
<tr>
<td>instruction fetch</td>
<td>instruction stream</td>
<td>none*</td>
</tr>
<tr>
<td>state address computation</td>
<td>instruction stream</td>
<td>none*</td>
</tr>
<tr>
<td>data address computation</td>
<td>instruction stream</td>
<td>none*</td>
</tr>
<tr>
<td>data meet PU + other overhead</td>
<td>instruction stream</td>
<td>none*</td>
</tr>
<tr>
<td>I / O to / from off-chip RAM</td>
<td>instruction stream</td>
<td>none*</td>
</tr>
<tr>
<td>inter PU communication</td>
<td>instruction stream</td>
<td>none*</td>
</tr>
<tr>
<td>message passing overhead</td>
<td>instruction stream</td>
<td>none*</td>
</tr>
<tr>
<td>transactional memory overhead</td>
<td>instruction stream</td>
<td>none*</td>
</tr>
<tr>
<td>multithreading overhead &amp; cache misses</td>
<td>instruction stream</td>
<td>none*</td>
</tr>
</tbody>
</table>

---

**The History of Computing**

*Prototype 1884: Herman Hollerith - the first reconfigurable computer*

1899 used for US population census
Size: like about 3 refrigerators
The first Xilinx FPGA came 100 years later

---

**Early LUT**

field-programmable: manually swapping plug boards non-volatile configuration memory

60 years later: RAM available - e.g. ferrite core (motivation for von Neumann machine paradigm)

---

**60 years later**

much larger than 3 refrigerators von Neumann syndrome - just for a few ballistic tables: the „von Neumann“ paradigm
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Single Paradigm (from the Mainframe Age) is obsolete

<table>
<thead>
<tr>
<th>term</th>
<th>controlled by</th>
<th>execution triggered by</th>
<th>paradigm</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>program counter (at ALU)</td>
<td>instruction fetch</td>
<td>instruction stream</td>
</tr>
<tr>
<td>DPU*</td>
<td>data counter(s) (at memory)</td>
<td>data arrival*</td>
<td>data-stream</td>
</tr>
</tbody>
</table>

+ New Machine Model for FPGAs

- Twin paradigm

Acceleration Mechanisms

Accelerate tasks by streaming

MTSD structured computation: streaming computations across a long array before storing results in memory.

Can achieve 100x in improved use of memory.

- parallelism by multi bank memory architecture
- auxiliary hardware for address calculation
- address calculation before run time
- avoiding multiple accesses to the same data
- avoiding memory cycles for address computation
- optimization by storage scheme transformations
- optimization by memory architecture transformations

Programming Model: Flowware

- Pros for streaming
  - Streamlined, low-overhead communication
  - (More) deterministic behaviour
  - Good match for many simple media rich applications
- Cons
  - control-dominated applications
  - shunt yard problem

We've to find out which applications types and programming models Students should exercise for the flowware approach

The Machine Model Dichotomy

von Neumann versus data stream machine

1st Step:
The Generalization of Software Engineering
Reiner Hartenstein. Informatik Department, TU Kaiserslautern, Germany

program source | result
---|---
Software | instruction streams
Flowware | data streams
Configware | datapath structures configured

CPU-centric Flat World Model
Aristotelian model
(CS: introduced in the 40ies)

CPU-centric, sequential-only, mind set
but no hardware know-how

This Software-only world model is obsolete
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**The Language and Tool Disaster**

- Software people don’t speak VHDL
- Hardware people don’t MPI nor OpenMP
- Bad quality application development tools
- 86% designers hate their tools (N. Connnor et al.: FPGAs for Dummies)
- Comprehensibility barrier between procedural and structural mind set

**Dual Paradigm Mind Set: an old Hat**

(mapping from procedural to structural domain)

We need

- Software mind set: instruction-stream-based:
  - flow chart → control instructions

- Mapped into a Hardware mind set:
  - action box = Flipflop, decision box = (de)multiplexer

1972: C. G. Bell et al.: The Description and Use of Register-Transfer Modules (RTM’s); IEEE Trans-C21/5, May 1972

**POIIP: Loop turns into Pipeline**

(reconfigurable) DataPath Unit:

- complex loop body
- nested loops
- (mapped into)
- complex rDPU or pipe network inside rDPU


**Locality Awareness is essential for Flowware**

Programmer instruction for Reconfigurable Computing:

- Software: by addresses, read from instruction
- Flowware: by wire (configured before run time)

**Development with VHDL is expensive**

- Unlike software, FPGAs do not offer forward/backward compatibility
- FPGA: low technology maturity, small user base, compared to software
- FPGA’s Achilles’ Heel is their long development time: Low level HDLs (VHDL/Verilog) are still dominant

**Locality Awareness**

- How data are moved
- Software: by addresses, read from instruction
- Flowware: by wire (configured before run time)
- space to time mapping
- time to space mapping

**Conclusion**

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Productivity vs. Efficiency

HDLs: zero ease of use!!!

"Adoption of VHDL was one of the biggest mistakes in the history of design automation, causing user and EDA vendors to waste hundreds of millions of dollars."


"The Plight of EDA" [R. N.]

how to hide the ugliness from the user [R. Newton]

Fig. 3. Productivity graph of HLLs

Language-of-the Year Phenomenon

[R. Newton]

Digital Simulators in Use

early 1970’s

early 1990’s

HDL Cadence

VHDL

Texas Instruments

Silicon

HDL Cadence

Fig. 2. Language-of-the-Year Phenomenon

HDLs: zero ease of use!!!

HDL programming models

Fig. 1. Classification of HLLs programming models

Understanding Heterogeneous Systems

We must change how programmers think

Intermodule Communication reduces Computational Efficiency

Understanding streams through complex fabrics needed

Efficient Distribution of Tasks being memory limited

Focusing on memory mapping issues and transfer modes to detect overhead and bottlenecks

Layers of Abstraction and Automatic Parallelization hide critical sources of, and limits to efficient parallel execution

essential: awareness of locality.

Understanding Architecture

NoC Projects

Industry faces "platform collision"

Which platform technology will win?

ASIC, ASSP, FPGA, MCU or IP core?

"It’s not clear, all may coexist"

Battles will get further interesting if/when the parallel programming crisis is over

NoC research: world-wide >60 projects

>60 NoC Projects

Jh-Sheng Shen, Pao-Ann Hsiung (editors); Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication; Information Science Reference, Hershey, USA, April 1, 2010

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**Triple paradigm systems?**

- **Hardwired accelerators**
- **Reconfigurable accelerators**
- **Self-reconfigurable neurocomputing**

**Self-organizing Fault Tolerance**

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**What ANNs can do**

- Single hidden layer enough
- Classification
- Defects-Tolerant Accelerators

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**Defects-Tolerant Accelerators?**

- No need to identify disable just learn
- Denoise of hardware NNs:
  - SVM algorithmic;
  - application scope
  - “killer micro”

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**Reconfigurable Neuro Computing**

- Generalization of the LUT
- from Boolean Algebra to Steinbuch Algebra
- from Reconfigurable Computing to Reconfigurable Neuro Computing (RNC)
- Field-Programmable Neuron Array (FPNA)

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**Conclusions**

- To avoid future unaffordability of our Cyber Infrastructure we need a Massive Migration Effort
- Legacy Software creates Masses of Jobs for Decades ... achieves much more than most Climate Protection Proposals
- We must start this Campaign as long as we can afford it
- We have to activate the Public and the Media, currently fully ignoring this worldwide vital issue

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**RC is the Silver Bullet**

A fascinating Challenge to reach new Horizons of research.

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Obrigado!
http://hartenstein.de/bio.pdf
reiner@hartenstein.de

Rewriting needed anyway

Backup for Discussion

Strong Synergy

• Rewriting of software needed anyway: for the survival of the µP industry (to cope with the transition to manycore)

• Extended scope of Software Rewriting: to save energy by orders of magnitude

• different from "classical" green computing

normal Hype Curve

[Olivier Temam: The Rebirth of Neural Networks; 37th ISCA, June 19-23, 2010, Saint-Malo, France]

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Normal Hype Curve

Neural Network Hype Curve

stopped Funding for 15 Years (world-wide)

Marvyn Minski's blind alarm

SVM: Support vector machines: set of supervised learning methods to analyze data and recognize patterns
Complex Programmability Crisis

Concurrent vs. FPGA Programming
Fine Grain vs. Coarse Grain Programming vs. hetero Programming
Acceleration needs an in-depth Application Study: requires more Programming Effort
Survey urgently needed: Manpower required!

Processor inside FPGA vs. FPGA inside Processor: EPP
Xilinx: Extensible Processing Platform™
→ totally changed concept
device more like heterogeneous SoCs:
significant benefits for HPC applications:
not hardware centric:
FPGAs became software-centric:
→ EDUCATION !!!!

Structured ASICs like eASIC are based mostly on FPGA-like architecture with special configuration mechanism to program at mask level: not re-programmable (more performance for less cost).

RTL Programming to ASIC / ASSP
Platform-Language of Silicon: attractive for IP providers
Tools-Path to ASICs/ASSPs, across FPGAs
RTL is inherently parallel, mapped application are automatically optimally parallelized by CAD tools.
now ESL (Electronic System Level) bridging HDL and ANSI C/C++ (at industrial level)

Battle between FPGAs vs MPSoC:
it is RTL vs Software programming.

Design methods and tools
Tools have impact on designer productivity
covers all the main steps of synthesis and analysis, including:
capturing domain-specific knowledge, profiling,
design space exploration, multi-core partitioning,
(H/SoS)system partitioning, data representation optimization,
static and dynamic reconfiguration, optimal custom instruction set generation,
functional simulation, programming mixed HW/SWsystems,
ensuring effective cross-boundary communication (another challenging issue).

Graphical/Dataflow Languages
Evaluation Metrics
We should have a look at DSPlogic

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Evolve the Software Ecosystem

The entire software ecosystem needs to evolve (including curricula):
- O/S
- Libraries
- SW development environments
- compilers and languages
- additional data structures and storage organization
- the new distributed memory discipline
- additional levels of parallelism: chaining, pipelining, systolic, super-systolic, wavefront arrays
- Legacy scientific applications: predominantly sequential

The wrong Direction: by Herd Instinct?

The transition from machine level to higher level languages led to the biggest productivity gain ever made

It's alarming that today's megabytes of code are compiled from languages at low abstraction levels (C, C++, Java)

Java is a religion – not a language (Ray Pompl)

The biggest productivity gain ever made was the transition from machine level to higher level languages

Tools for Team Design

28-nm FPGAs deliver the equivalent of a 20- to 30-million gate ASIC.

FPGA design tool operation in a reasonable time impossible

Widening the Semantic Gap

unnecessary complexity inside

The PISA project

>15,000 speed-up factors are not new by avoiding the von Neumann paradigm

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Danger of the Situation
Unnecessary Complexity
1963
2010
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Parallel Programming Gap
Unnecessary Complexity
Ability to Master Complexity
1963
2010
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Scientific Revolutions
1st Newtons Law
( inertia): „people do not change direction”
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>40 years Software Crisis
In 1955, Parkinson could not have foreseen the impact of software.
The size of bureaucracy is independent of the amount of real work to be done.
Anthony Berglas 2008: Why it is Important that Software Projects Fail

Apropos Herd Instinct
Some Programming Languages
G. Bell: „People do not change Direction“ ( follow Herd Instinct)
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Architecture visible
to the programmer
The software programming model:
Which hardware architecture parts are visible and under the programmer’s direct control?
The RC programming model:
how the programmer can control data transfers between FPGA, onboard memory, the microprocessor and its memory

Keynote, The 1st Brazilian-German Workshop on Micro and Nano Electronics (BGME’2010), October 6 - 8, 2010, Porto Allegre, RS, Brazil
The Human Brain ...

"The human brain needs only a few watts for about 10,000,000,000,000,000 (ten million billion) compute operations per second. Von-Neumann-paradigm-based it would need more than a MegaWatt, the electric power needed for a small town and it would sizzle off in a fraction of a second." [Yield Fusion]

System on a Chip development: Yesterday's chip is today's functional block!

New design methodologies needed

SoC - System-on-Chip

System on a Chip development: Yesterday's chip is today's functional block!

New design methodologies needed

Vertical Disintegration

1960  [Courtesy Manfred Glesner] 200X

Participants in the Value Chain

Twin paradigm systems

CPU: "Central Processing Unit"

However, it needs accelerators

"Central": it controls (almost) everything

ASIC: 3%

FPGA: 97%

[Dataquest, 2009]

[Courtesy Manfred Glesner]

Neural Network Hype Curve

(Olivier Temam, 2010)

(Olivier Temam: The Rebirth of Neural Networks; 37th ISCA, June 19-23, 2010, Saint-Malo, France)