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An Embedded Accelerator for Real Time Image Processing

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Abstract

The paper presents an embedded reconfigurable accelerator, called Xputer, comprising a novel kind of sequencer hardware (Data Sequencer). For many real time signal processing, multimedia, and other high-performance applications this new data-driven architecture increases the performance of a single processor system enourmously by integrating it as a co-processor for accelerating computation-intensive parts of an application. Here the reconfigurable architecture incl. programming environment is described. Its use is illustrated with an automotive application requiring real time image processing.

1. Introduction

Many applications in signal and image processing require fast access to structured data. Most of the time, the data structures are arrays, either of simple scalar values or arrays of records. In many algorithms (e.g. FFT, or FIR filtering), the access sequence to the data is already known at compile time, because the index computations to the array elements are done by nested loops, which do not depend on the actual data values. This is the reason, why most digital signal processors [16] [17] [18] [19] contain independent address generating ALUs. They are used to compute the addresses of data for future use in parallel to the data manipulations on already fetched data. Typically, these address generators are capable to produce a linear address sequence with constant offsets between subsequent addresses, cyclic or modulo addressing for cyclic buffers, and bit-reversed addressing for FFT-type applications. In addition to linear address sequences, it is capable to access data in two-dimensional arrays from a single set of parameters. All of the address generators described above are capable to provide addresses for scalar values only. The frequent cases, where an algorithm requires access to structured data (e.g. a subarray moving as a sliding window across the whole data array in two-dimensional FIR filtering) require a new setup of the address sequence parameters quite often. This is because these address generators cannot make use of the hierarchy information, where a simple data access sequence (the accesses to the subarray or record elements) is repeated in a regular manner to access a large amount of structured data.

The new paradigm of Xputers [1] [6] [7] is based on reconfigurable logic supporting structural programming like the rALU concept (reconfigurable ALU) [6] or the rDPA approach (reconfigurable data path array) [12] [13]. This data-driven paradigm provides an address generating device to support structured data access for multi-dimensional arrays. We call this device Generic Address Generator, because it is used to produce generic address sequences ahead of the data manipulations without consuming instruction or memory bandwidth apart from a few parameter transfers. Multiple Generic Address Generators combine to a Data Sequencer, which controls data manipulations by the sequence in which data arrives at the rALU. An Xputer can be integrated as accelerator within a workstation environment for computation-intensive parts of an application.

For this new class of hardware platforms a new class of compilers is needed, which generate both, sequential and structural code: i. e. partitioning compilers. This paper introduces a parallelizing compilation method with two levels of partitioning: host/accelerator partitioning and a structural/sequential partitioning (second level).

The following section introduces the target hardware. In the second chapter the methods of the programming environment are sketched. The real time use of the Xputer as embedded accelerator is demonstrated by an application example from high-speed image analysis for automotive applications.

2. The Target Hardware

The target hardware consists of a host workstation that uses the Xputer [5] [6] [7] as a universal hardware accelerator (see figure 1). With Xputers the highest speed-up is obtained for algorithms, which iterate the same set of operations over a large amount of data. Such operations are mapped onto a reconfigurable parallel arithmetic-logic unit (rALU). All input and output data to the complex rALU operations is buffered in a scan window (SW), which is a kind of smart register file, the location sequence of which in memory space is determined by a data sequencer. All data in the scan