

Reconfigurable HPC¹: torpedoed by Deficits in Education ?

(keynote address²)

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Abstract. Currently there is a deep chasm between Reconfigurable Computing (RC) and the way, how "classical" CS people look at parallelism [1]. The situation is comparable to the well-known hardware / software chasm. In education until recently RC has been subject of embedded systems or SoC design within EE departments, whereas most classical CS departments have ignored the enormous speed-up opportunities which can be obtained from this field. Only a few departments provide special courses mostly attended by a small percentage of graduate students. Conferences like ISCA stubbornly refused to include RC and related areas in their scope. Also many major players in the IT market have mainly ignored this area.

Since some months ago this situation is on the way to be changed. An increasing number of colleagues from classical parallel computing or supercomputing communities is going to be ready to discuss fundamental issues with us [2] [3]. Last year, Intel Research at Hillsboro, Ore, held a major internal workshop on RC. It has been told, that also Microsoft has held an internal workshop on this area. Other major players have already joined this movement, like Hewlett Packard, IBM, infineon, Motorola, Sony, ST microelectronics, Texas Instruments, Toshiba, and others. A major break-through also in CS education is overdue. All scientific and know-how ingredients needed are available - ready to be integrated in all CS curricula: software / configware co-compilation [4] [5], software to configware migration [6] [7], mapping applications onto morphware [6] [7] [8] [9], architectural resources for data-stream-based anti machines [10] [11] [12], and many others. Not only FPGAs, but also coarse grain datapath array platforms are available commercially along with application development tools [13].

The new road map is based on the duality of an instruction-stream-based mind set, and a data-stream-based mind set [1] [12] [14] [15]. Not only the HPC community urgently needs to benefit from a curricular revision. A rapidly increasing percentage of

1) High Performance Computing

2) prepared for the first International Workshop on Reconfigurable Systems for HPC (RHPC), July 21, 2004, held in conjunction with the 7th International Conference on High Performance Computing and Grid in the Asia Pacific Region (HPC Asia 2004), July 20 - 22, 2004, Omiya Sonic City (Tokyo Area), Japan

programmers implements code for embedded systems. However, most CS graduates are not qualified for this changing labour market. With their procedural-only mind set they cannot cope with hardware / configware / software partitioning. Currently such tasks are mainly carried out by EE professionals. In order not to loose this competition, and, to avoid a disaster for future CS graduates looking for their first job, CS departments have to wake up. Here we have a good chance to become successful trailblazers by forming a RC old boys' network together with colleagues from "classical CS", organized like the Mead & Conway movement more than 20 years ago [16].

References

- [1] R. Hartenstein (invited paper): The Digital Divide of Computing; Proc. 2004 ACM Int'l Conf. on Computing Frontiers (CF04); Ischia, Italy, April 2004
- [2] R. Hartenstein (keynote address): Software or Configware? About the Digital Divide of Computing; IPDPS 2004, Santa Fe, NM, April 2004
- [3] R. Hartenstein (invited paper): Data-Stream-based Computing and Morphware; Joint 33rd Speedup and 19th PARS Workshop (Speedup / PARS 2003), Basel, Switzerland, March 2003
- [4] K. Schmidt et al.: Combining Structural and Procedural Programming by Parallelizing Compilation; Proc. 1995 ACM Symp. on Applied computing, Nashville, TN., Feb 1995
- [5] J. Becker et al.: Parallelization in Co-Compilation for Configurable Accelerators; Proc. ASP-DAC'98, Yokohama, Japan, Febr 1998
- [6] R. Kress et al.: A datapath Synthesis System for the reconfigurable Datapath Architecture; Proc. ASP-DAC 1995, Chiba, Japan, August 1995
- [7] U. Nageldinger et al: KressArray Xplorer: a new CAD Environment to optimize Reconfigurable Datapath Arrays; Proc. ASP-DAC 2000, Yokohama, Japan, Jan 2000
- [8] R. Hartenstein (embedded tutorial): A decade of Reconfigurable Computing: a Visionary Retrospective; Proc. DATE 2002, Munich, Germany, March 2002
- [9] R. Hartenstein (embedded tutorial): Coarse Grain Reconfigurable Architectures; Proc. ASP-DAC 2001, Yokohama, Japan, Jan 2001
- [10] A. Hirschbiel et al.: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware; Proc. InfoJapan'90, Tokyo, Japan, 1990
- [11] Invited reprint of [10] in: Future Generation Computer Systems 7 91/92, North Holland Publ.
- [12] M. Herz et al. (invited paper): Memory Organization for Data-Stream-based Reconfigurable Computing; Proc. IEEE ICECS 2002, Dubrovnik, Croatia, Sept 2002
- [13] <http://pactcorp.com>
- [14] J. Becker et al. (solicited paper): Configware and morphware going mainstream; Journal of Systems Architecture, vol. 49, Issue 4-6 (Sept 2003)
- [15] R. Hartenstein (invited chapter): Morphware; in: A. Zomaya (editor): Handbook of Innovative Computing; LNCS series, Springer Verlag Heidelberg/New York, 2004
- [16] R. Hartenstein (opening keynote): Are we ready for the Breakthrough ?; 10th Reconfigurable Architectures Workshop 2003 (RAW 2003), Nice, France, April 2003